Instruction Manual

Tektronix

P6467
High-Speed Probe Adapter

070-9176-00

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Do Not Operate Without Covers

To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse

To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions

To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere

To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Avoid Exposed Circuitry

To avoid injury, remove jewelry such as rings, watches, and other metallic objects. Do not touch exposed connections and components when power is present.

Product Damage Precautions

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Immerse in Liquids

Clean the probe using only a damp cloth. Refer to cleaning instructions.

Safety Terms and Symbols

Terms in This Manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:

DANGER
High Voltage

Protective Ground
(Earth) Terminal

ATTENTION
Refer to Manual

Double
Insulated

Overvoltage Category

Overvoltage categories are defined as follows:

CAT III: Distribution level mains, fixed installation

CAT II: Local level mains, appliances, portable equipment

CAT I: Signal level, special equipment or parts of equipment, telecommunication, electronics

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

The P6467 Instruction Manual is intended to help you setup and use the P6467 High-Speed Probe Adapter to acquire data from a system-under-test through a DAS/NT, DAS/XP, or a TLA 520 logic analyzer. The manual contains the following sections:

- Getting Started provides an overview of the P6467 adapter assembly, a list of accessories, installation and configuration instructions and a brief function check procedure.
- Operating Basics provides functional overview of the P6467 adapter assembly. It describes the connectors and clock jumpers on the probe.
- Reference provides reference information on acquiring data and using software commands to transfer acquired data to a host and saving acquired data in a reference memory.
- Specifications describes the specifications of the P6467 Probe.
- Performance Verification provides procedures for verifying the performance requirements of the P6467 Probe.
- Maintenance describes procedures for inspecting, cleaning, and servicing the P6467 Probe. It also includes troubleshooting procedures and a brief theory of operation.
- Replaceable Parts lists the replaceable parts of the P6467 Probe and the probe accessories. It also provides an exploded view of the probe.
- The Appendix provides pinout tables of the P6467 Probe and brief information on the P6467 Test Board.

Definition of Terms

You may encounter the following terms throughout this manual:

- 92A96 Module. The 92A96 Data Acquisition Module is a 96-channel, 100 MHz data acquisition module. It is available is different memory depths. the 92A96 Module is part of the DAS or TLA logic analyzer family.
- 92C96 Module. The 92C96 Data Acquisition Module is a variation of the 92A96 Module. The 92C96 Modules can be easily upgraded for more memory through upgrade kits.

  The terms 92A96 and 92C96 are used interchangably throughout this manual.

- Logic Analyzer. The term logic analyzer is used with either DAS/NT, DAS/XP, or TLA 520 Logic Analyzers.
- Two-Card Module. A two-card module refers to a 92A96 Module with two individual 92A96 circuit boards or modules. The two cards form a 192-channel wide data acquisition module.
- Three-Card Module. A three-card module refers to a 92A96 Module with three individual 92A96 circuit boards or modules. The three cards form a 288-channel wide data acquisition module.

Related Documentation

In addition to this manual you may need to refer to the following documents while using the P6467 adapter assemblies:

- *92A96 & 92C96 Module User Manual*. This manual describes the 92C96 and 92A96 Modules and how to set up, acquire, and display data with the acquisition module.
- *DAS System User Manual*. This manual describes how to use the DAS/NT or DAS/XP digital analysis systems to acquire data with the 92A96 Data Acquisition Modules.
- *TLA 510 & TLA 520 User Manual*. This manual describes how to use the Tektronix Logic Analyzers to acquire and display data with the 92A96 Data Acquisition Modules.
- *DAS 9200 Programmatic Command Language User Manual*. This manual describes how to use the Programmatic Command Language through GPIB or 92LAN to control the DAS from a remote location.
- *92LANP Instruction Manual*. This manual describes how to communicate with a DAS mainframe through a local area network (LAN).
- *DAS 9200 Acquisition and Pattern Generation Files User Manual*. This manual describes the structure of acquisition data files. You may need to access this information if you intend to manipulate acquired data on a host computer.
- *LA–Offline User Manual*. This manual describes how to use the LA-Offline application software to analyze logic analyzer data on a host computer.

Getting Started

This chapter provides an overview of the P6467 High-Speed Probe Adapter. It also describes the accessories available with the P6467 Probe as well as installation and configuration instructions.

Product Description

The P6467 High-Speed Probe Adapter is designed for the DAS/NT, DAS/XP, or TLA 500 series logic analyzers with the 92A96 or 92C96 Data Acquisition Modules. The probe provides high-speed data acquisition and logic analysis for synchronous clocking applications. The probe has the following key features:

- Synchronous data acquisition of speeds of up to 195 MHz (DIV2 mode)
- Synchronous and asynchronous acquisition of data of speeds up to 100 MHz (NORM mode)
- Quick connection of data and clock signals

You can configure the probe to operate in one of two modes, DIV2 and NORM. When you use the probe in the DIV2 mode, the probe effectively doubles the speed and memory depth of a 92A96 Module. The NORM mode lets you acquire data synchronously and asynchronously in speeds up to 100 MHz.

Each probe connects to the system-under-test through two connectors. Each probe acquires 48 data signals and two clock signals through two flexible circuit board cables.

The probe comes with application software that lets you create a reference memory from the acquired data and transfers the data to a host. The data that is acquired by a pair of 92A96 modules is merged into a single column for analysis on the host. You control the application software using the EXEC Programmatic Command Language (PCL) command from a host through GPIB or 92LANP.

The application software also contains sample setups that you can use to help set up the logic analyzers. These setups can help you reduce the amount of time required to set up menus for certain applications.

In addition to viewing the data on a host from the logic analyzer, you can also view the data on the host with the Tektronix LA-OffLine software for off-line data analysis.

Accessories

The following standard accessories come with the P6467 High-Speed Probe Adapter (refer to *Replaceable Parts* on page 55 for part number information):

- Probe Power cable
- Clock Distribution cable
- Master Clock Delay cable
- P6467 Instruction Manual
- P6467 Support Software
- 92LANP Application Software and manual

Installation

This section provides installation information for the probe. This section does not provide installation instructions for the 92A96 Modules. If you purchased a 92A96 Module with your P6467 probe, refer to the *DAS System User Manual* or to the *92A96 and 92C96 Module User Manual* for instructions to install a 92A96 Module in a DAS mainframe. Then return to this manual for instructions to complete the installation of your P6467 probe.

If you have a TLA 520 logic analyzer, the 92A96 Modules are already installed in the mainframe (system unit).

System Requirements

Before using the probe you must meet the following hardware and software requirements on your DAS or TLA systems:

- A DAS or TLA mainframe with System Software Release 3, Version 1.51 or higher.
- The *Remote Operation Support* optional system software.
- Two or more 92A96 Data Acquisition Modules installed in the mainframe
- The 92LANP application software or a DAS mainframe with a 92C02 GPIB/Expansion Module.

Configure and Install the Probes

Before you use the P6467 probe you must determine the operating mode and the clocking requirements for your application. The clocking requirements depend on the number of cards in your 92C96 modules. You must specify one P6467 probe as the Master Clock probe and set the jumpers accordingly. Figures 1 through 3 show the clock jumpering and probe connections for two single-card modules, two two-card modules, and two three-card modules respectively. The clock signals are shown in bold in the illustrations. Table 1 on page 6 shows the jumper settings when the probe is shipped from the factory.

Note that in each of the examples, the P6467 probe connected to the blue-labeled probe cables is defined as the Master Clock probe; your application may call for a different color-coded probe label.

If you have the module configuration as shown in Figure 1, the position of the MSTR CLK/CLK A jumper can be in either the MSTR CLK or the CLK A position. However, the jumper must be in MSTR CLK position for the Master Clock probe in two- and three-card modules as shown in Figures 2 and 3.

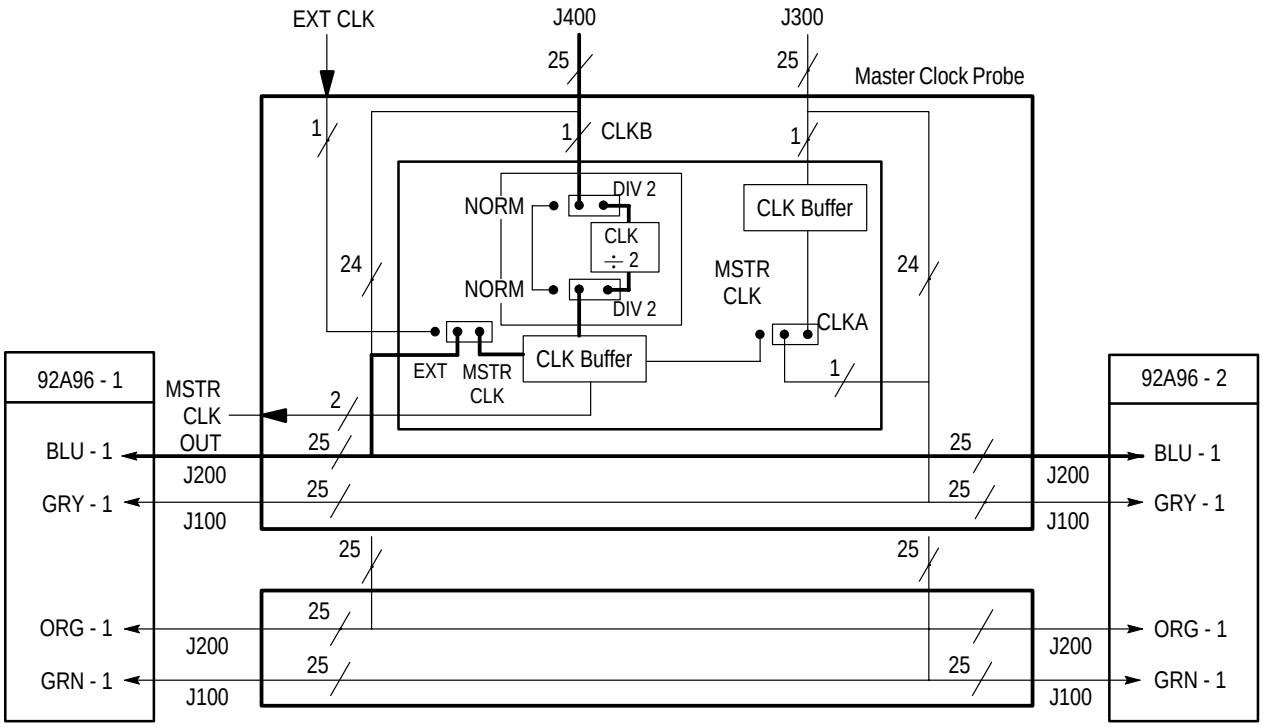


Figure 1: Probe Connections and Clock Jumpering for Two Single-Card Modules

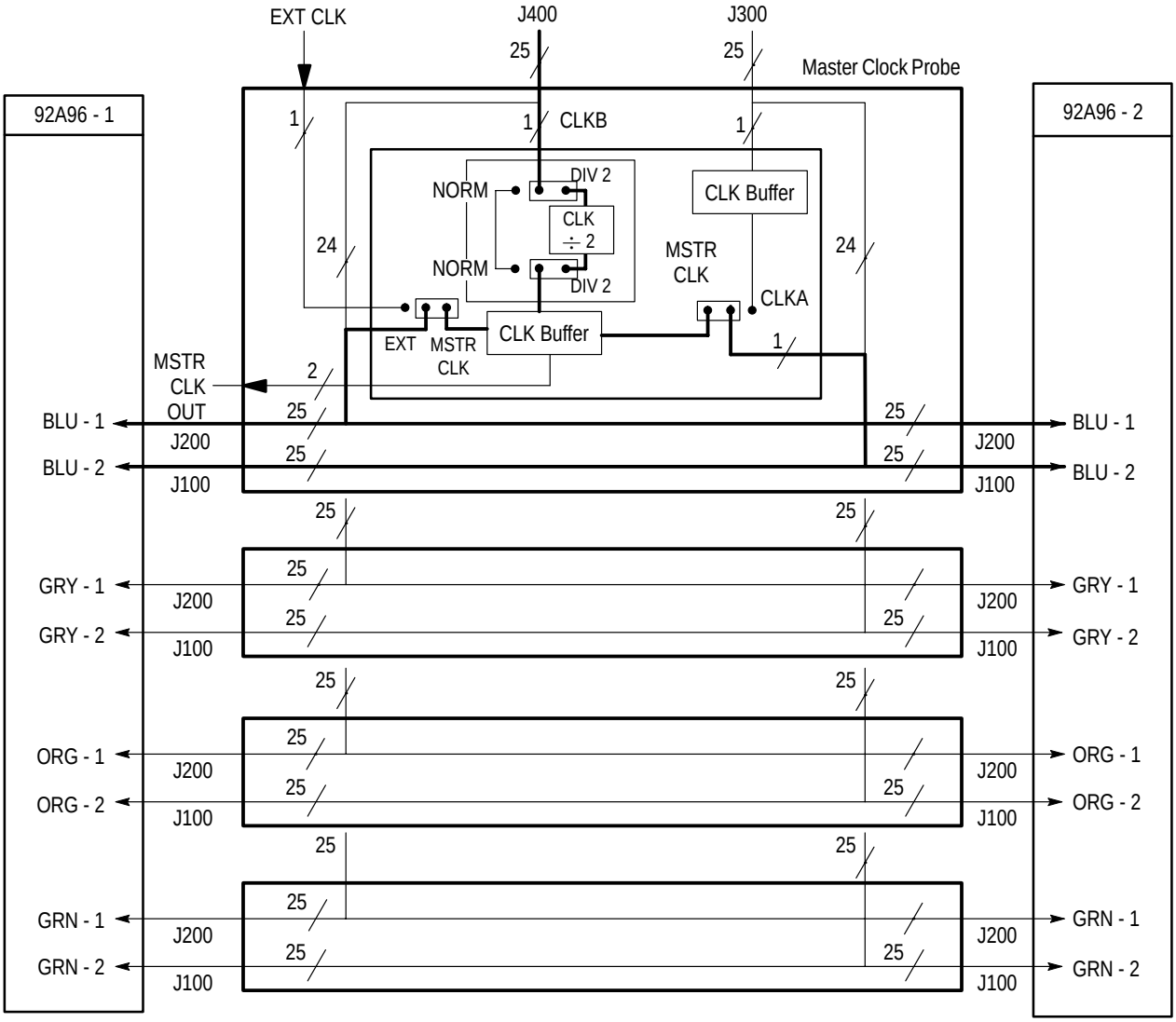


Figure 2: Probe Connections and Clock Jumpering for Two Two-Card Modules

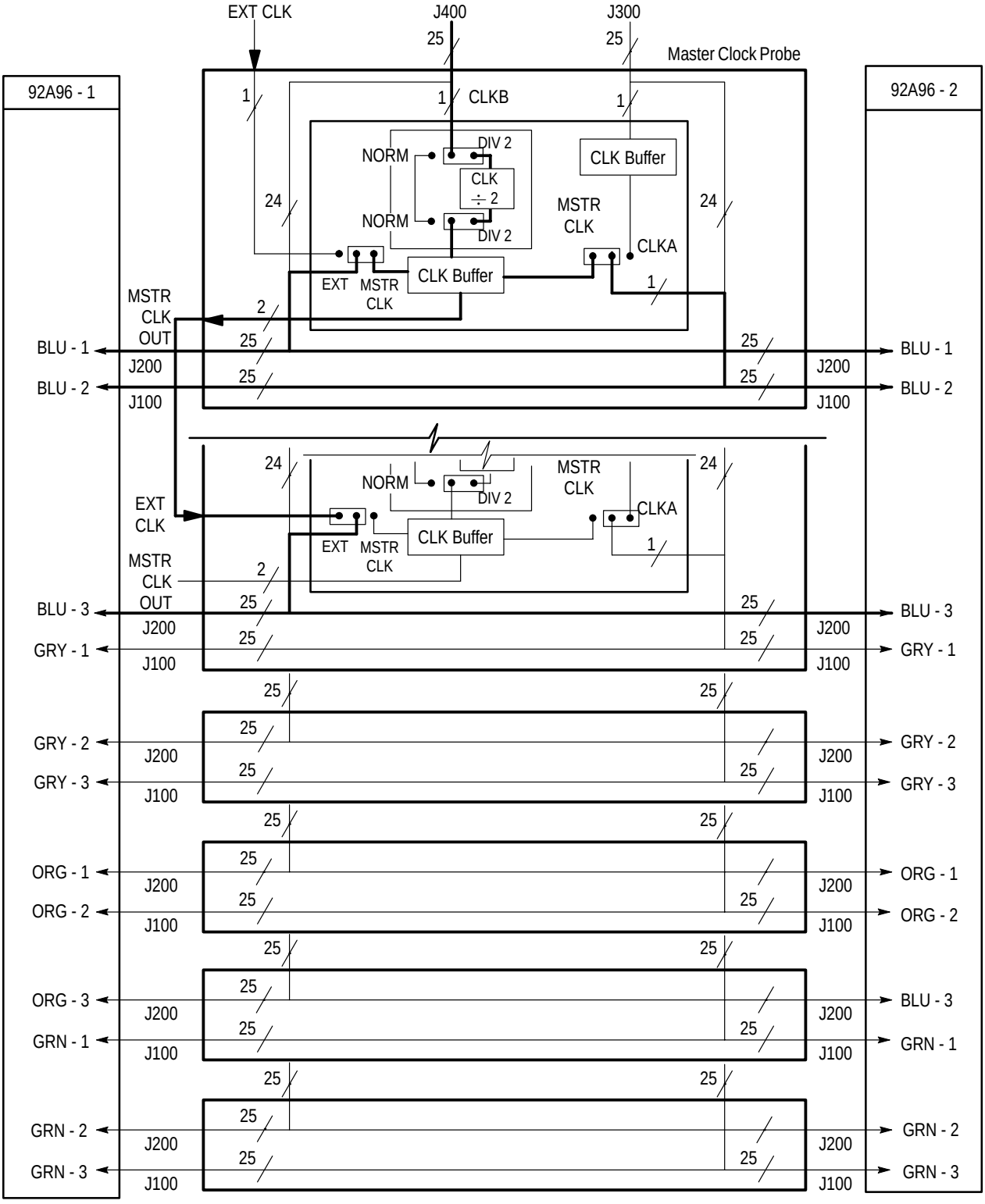


Figure 3: Probe Connections and Clock Jumpering for Two Three-Card Modules

Table 1: Factory Default Jumper Positions

P6467 Probe Jumper	Jumper Position
J1 (EXT/MSTR CLK)	MSTR CLK
J2 (NORM/DIV2)	DIV2
J3 (CLK A/MSTR CLK)	CLK A
J4 (DIV2/NORM)	DIV2

To set the clock jumpers on the Master Clock probe, you must remove the cover from the probe. To remove the cover, remove the two screws on each side of the probe. Figure 4 shows the locations of the jumpers on the probe. Note that it is only necessary to configure the jumpers on the Master Clock probe.

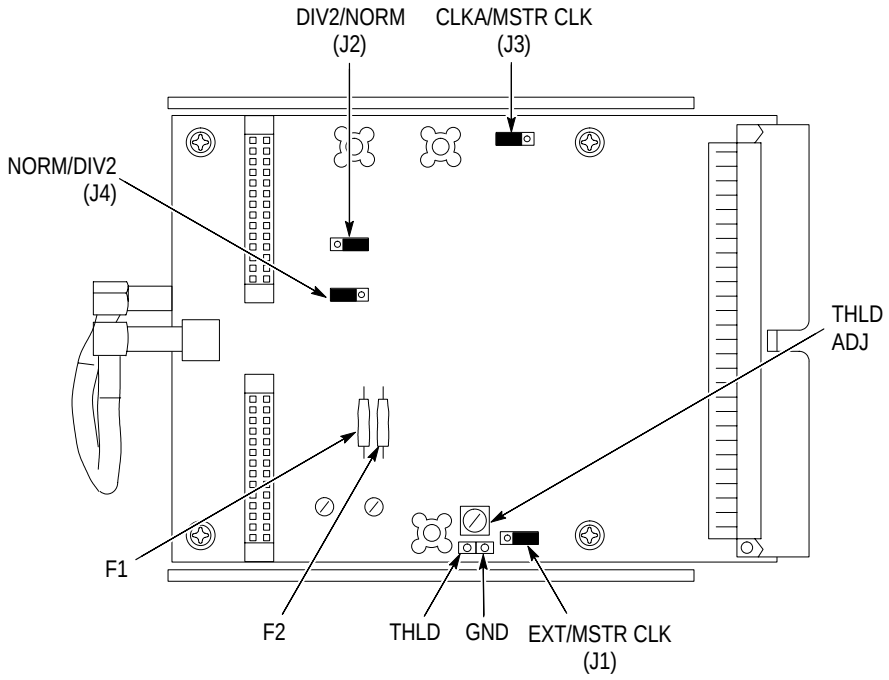


Figure 4: Clock Jumper Locations on the P6467 Probe

After determining the jumper locations on the probe, replace the probe cover and continue with the following steps:

1. Refer to Figure 5 and connect the probe power cable to the probes (each 92A96 Module can power two P6467).
   - **a.** Bend the power cable near the connector as shown.
   - **b.** Insert the power connector into the connector socket.

c. Use the tip of a pen or a small flat blade screw driver to push and lock the connector in place.

Refer to Figure 6 to disconnect the power cable from the probe.

2. Repeat steps 1a through 1c to connect the power cable to reach remaining P6467 probe.

3. Connect the power cable to the power connector on one of the 92A96 Modules in the logic analyzer.

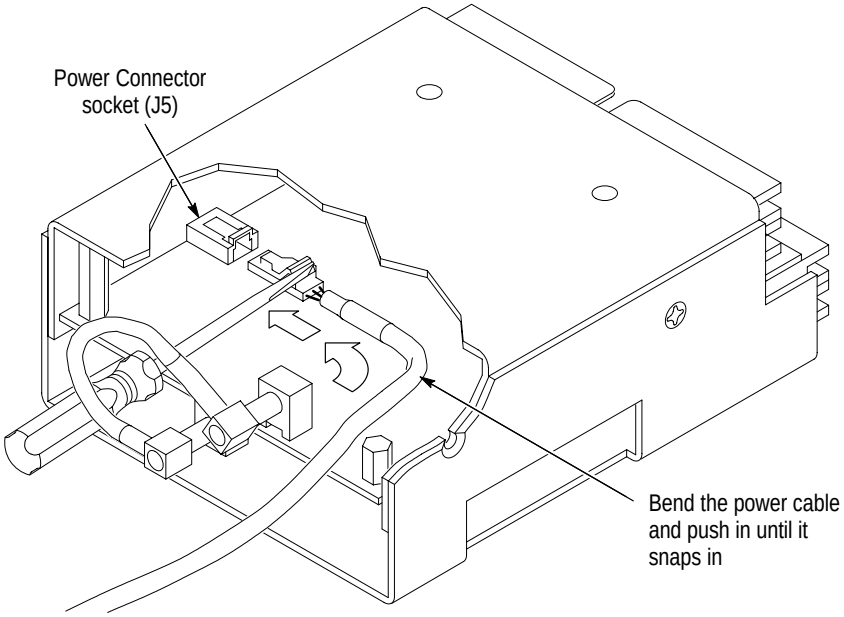


Figure 5: Connecting the Power Cable to the Probe

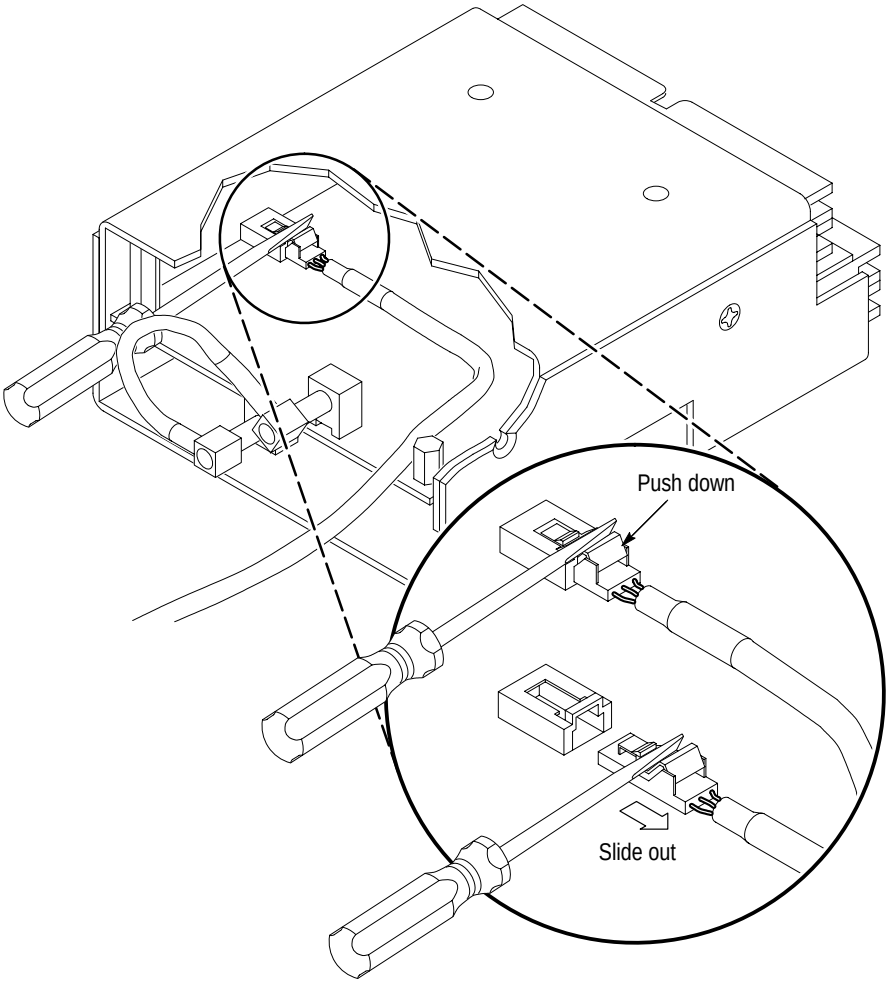


Figure 6: Disconnecting the Power Cable from the Probe

4. Connect the P6467 Probes to the 92A96 Probe Cables; if necessary, refer to Figures 1 through 3 on pages 3 through 5 respectively.

5. Connect the flexible leads of the probe to the system-under-test. Refer to Figure 7 to ensure that you properly connect the probe to the system-under-test (pin 1 of the probe to pin 1 of the probe connector).

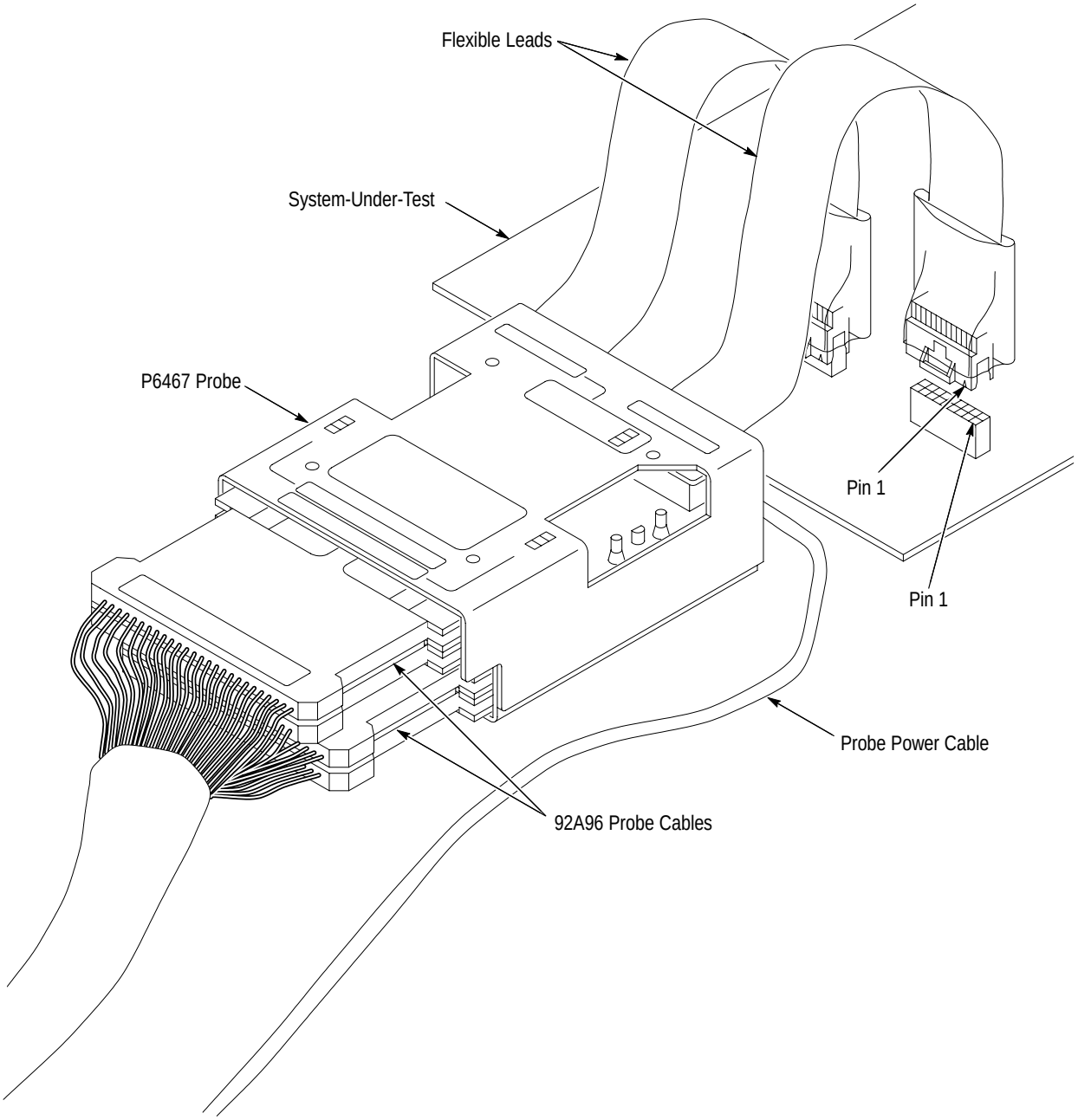


Figure 7: Connecting the Probe to the System-Under-Test

Install the Software Install the P6467 support software from the floppy disk using the Install Application selection from the Disk Services menu. Insert the floppy disk in the disk drive and follow the on-screen instructions to load the support software.

If you intend to use the 92LANP application software with the P6467 Support software, refer to the software installation instructions in the *92LANP Instruction Manual* to install the 92LANP software on the logic analyzer.

Configuration

Before you can acquire data with the P6467 probe you must determine how you want to use the probe, adjust the clock threshold voltage, and then set up logic analyzer to acquire data.

Configure the Probe Hardware

If you have not already done so, configure the clock jumpers on the probe following the instructions under *Configure and Install the Probes* beginning on page 3.

Adjust the Probe Threshold Voltage

You can adjust the threshold voltage of the clock inputs on the P6467 probe to meet the needs of your application. You only need to adjust the threshold voltage on the Master Clock probe. When shipped from the factory, the theshold voltage is set to 2 V.

To adjust the threshold voltage connect a digital voltmeter from test point THLD and the adjacent ground pin. The location of test point THLD is shown in Figure 4 on page 6. Adjust the threshold control (THLD ADJ) for a reading between –1.6 V and +2.6 V.

Set Up the Logic Analyzer

Setting up the logic analyzer consists of defining the Setup menus. The P6467 software contains an example of a setup file that you can restore from the hard disk.

The following steps summarize the basic setups, if necessary, refer to the *92A96 & 92C96 Module User Manual* for detailed information on using the Setup menus of the logic analyzer.

1. Use the System Configuration menu to define the cluster setups.
   a. Separate the 92A96 Modules into two separate, one-card, two-card, or three-card modules.
   b. Specify a cluster for the modules.
2. Use the Cluster Setup menu to correlate the two modules and to define the signals between the two modules.
3. For each module, use the 92A96 Configuration menu to specify the acquisition memory depth.

4. For each module, use the 92A96 Channel menu to define the channel setups and the data and clock threshold voltages. Set the clock threshold voltage to **VAR –1.85 V** and the data threshold voltage to **VAR +1.90 V**.

5. For each module, use the Clock menu to define the clocking requirements. If you setup the probe for use in the DIV2 operating mode, set the Clock menu to **External**. Set up one module to clock on the rising edge of the clock (with no qualification) and set up the second module to clock on the falling edge of the same clock as the first module.

6. For each module, use the Trigger menu to define the data you want to acquire and to assert and monitor the signals defined in the Cluster Setup menu. Figure 8 shows an example of one of the Trigger menus (the Trigger menu must be the same for both modules in the module pair with the exception of the definition of the signals used between the two modules).

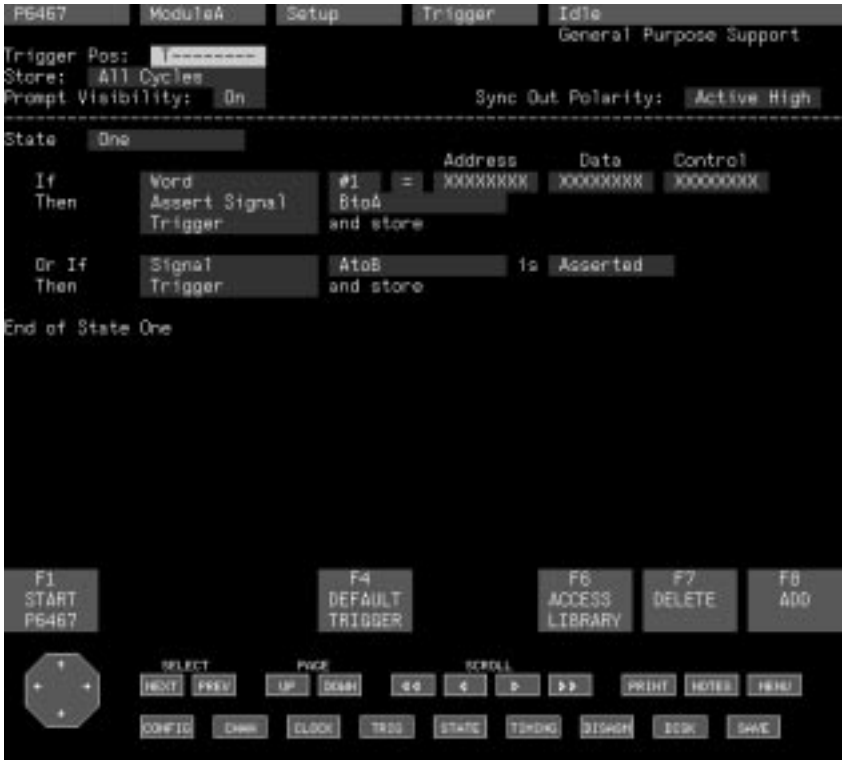


Figure 8: Sample Trigger Menu (First Module)

Figure 9 shows an example of the second Trigger menu of the module pair. The main difference between the two Trigger menus is the use of signals between the two modules. One module asserts the first signal and receives the second signal, while the other module receives the first signal and asserts the second signal.

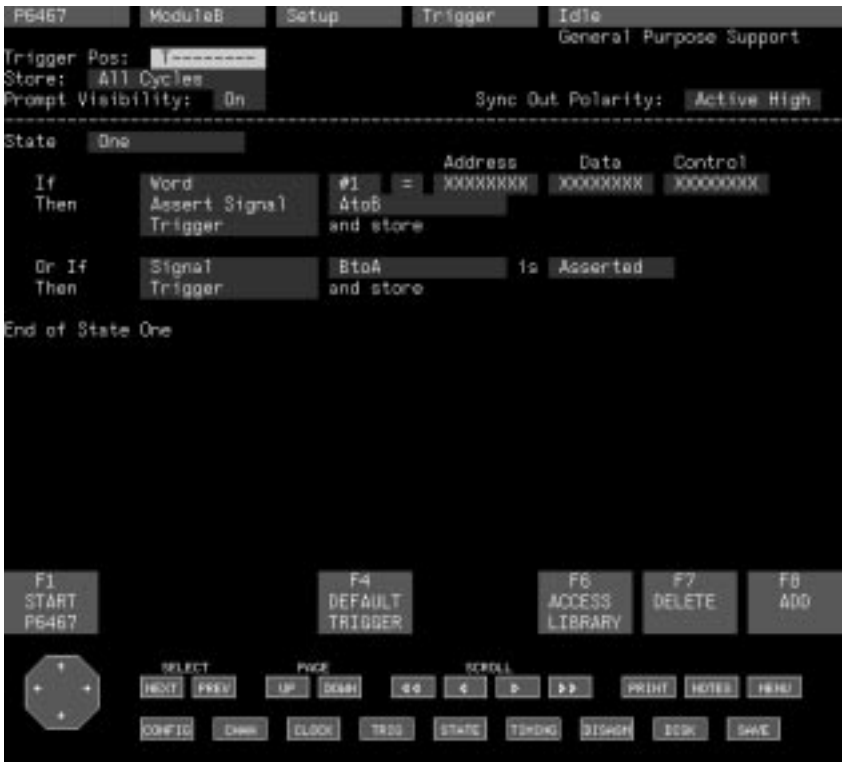


Figure 9: Sample Trigger Menu (Second Module)

Functional Check

You can verify the basic functionality of the probe by acquiring data and viewing it on the logic analyzer. You can use the following checks as an incoming inspection to determine if further testing or repair is necessary. The checks consist of connecting the probe to the P6467 Test Board and acquiring data through individual channels.

Equipment List

You will need the following equipment to perform the functional checks:

- TLA 520 Logic Analyzer, DAS/NT, or DAS/XP Logic Analyzer with two 92A96 or 92C96 Data Acquisition Modules
- Two sets of coaxial probe cables (Tektronix part number 198-5761-XX) or two sets of standard 92A96 probe cables
- One P6467 High–Speed Probe Adapter with Probe Power Cable
- P6467 Test Fixture (Tektronix part number 067-0262-XX)
- A pulse generator capable of supplying a 20 MHz, 0 to 3 V signal into 50 Ω, a 50% duty factor, a 1 to 4 ns rise time, and a complementary output
- One 42-inch 50 Ω coaxial cable (Tektronix part number 012-0057-01)
- One 20-inch 50 Ω coaxial cable (Tektronix part number 012-0076-00)
- Two 3 mm male-to-female BNC adapters (Tektronix part number 015-1018-XX)

Functional Check Setups

The following steps describe the setups necessary to perform the functional checks. The procedures assume that you are starting the checks with the probes disconnected from the logic analyzer and that the logic analyzer is powered off. The procedures also assume that you will use the setups stored on the hard disk from the P6467 Support Software.

1. Remove the cover from the P6467 Probe and set jumpers to the positions indicated in Table 2.

Table 2: Jumper Positions for Functional Checks

P6467 Probe Jumper	Jumper Position
J1 (EXT/MSTR CLK)	MSTR CLK
J2 (NORM/DIV2)	DIV2
J3 (CLK A/MSTR CLK)	CLK A
J4 (DIV2/NORM)	DIV2

2. Connect the blue-labeled probe cables from the two 92A96 modules in the logic analyzer and connect them to top pair of connectors (OUTPUT DATA A) on the P6467 Probe.

3. Connect the Probe Power cable from the power connector of one of the 92A96 Modules on the logic analyzer to the power connector on the P6467 Probe (if necessary refer to Figure 5 on page 7 for information on connecting the Power cable).

4. Power on the logic analyzer and the display terminal.

5. After the logic analyzer completes the power-on diagnostics, select the Save/Restore menu and restore the setup named P6467-PVD

   The restored setup has the menus already programmed for the functional checks. If the predefined setup does not match your hardware configuration, you will need to further modify the menus for your configuration (if necessary, refer to the *92A96 & 92C96 Module User Manual* for information on using the setup menus).

6. Connect the two 50 Ω cables to the outputs of the pulse generator.

7. Connect one of the 3 mm (SMA male-to-female BNC adapters to J1 and J13 of the P6467 Test Board.

8. Connect the two BNC cables to the 3 mm (SMA male-to-female BNC adapters.

9. Connect the shorter BNC cable from the complement output of the pulse generator to the clock connector (J13) on the P6467 Test Board.

10. Connect the longer BNC cable from the output of the pulse generator to the J1 connector on the P6467 Test Board.

11. Connect the INPUT DATA A flex lead of the probe to the 30-pin connector on the P6467 Test Board.

12. Set the pulse generator for a 20 MHz 0 V to +3 V output signal with a 50% duty factor and a 1 to 4 ns rise time (if necessary, use an oscilloscope to verify the setup).

13. Start the logic analyzer by selecting function key F1: START on the logic analyzer.

***NOTE**. If the logic analyzer displays a SLOW CLOCK message, check that all of the jumpers are in the correct positions on the probe and that you have correctly connected the clock signal from the pulse generator to the P6467 Test Board.*

---

14. The logic analyzer should trigger and display the State Display menu. The displayed data should resemble the following data:

```
0000 A0
              0000 00
0000 A0
              0000 00
0000 A0
              0000 00
0000 A0
              0000 00
```

The check verifies the functionality of the clock signal and the one data channel. You can verify the functionality of the remaining data channels by moving the pulse generator connection from J1 of the P6467 Test Board to one of the other channels and repeating the test. The acquired data in the State Display menu should track the data channel as you connect each data channel to the pulse generator output. Table 3 shows the expected data with respect to the data channel connection on the P6467 Test Board.

Table 3: Functional Check Data

P6467 Test Board Connection	INPUT DATA A or INPUT DATA B NORM Mode Data	INPUT DATA B DIV2 Mode Data
J1	0000 A0 0000 00	0000 A0 0000 A0
J2	0000 50 0000 00	0000 50 0000 50
J3	0000 0A 0000 00	0000 0A 0000 0A
J4	0000 05 0000 00	0000 05 0000 05
J5	A000 00 0000 00	A000 00 A000 00
J6	5000 00 0000 00	5000 00 5000 00
J7	0A00 00 0000 00	0A00 00 0A00 00
J8	0500 00 0000 00	0500 00 0500 00
J9	00A0 00 0000 00	00A0 00 00A0 00

Table 3: Functional Check Data (Cont.)

P6467 Test Board Connection	INPUT DATA A or INPUT DATA B NORM Mode Data	INPUT DATA B DIV2 Mode Data
J10	0050 00 0000 00	0050 00 0050 00
J11	000A 00 0000 00	000A 00 000A 00
J12	0005 00 0000 00	0005 00 0005 00

15. Disconnect the INPUT DATA A flex lead from the P6467 Test Board and connect the INPUT DATA B flex lead.

16. Disconnect the blue-labeled probe cable from the top connector of the P6467 Probe and connect them to the bottom connector (OUTPUT DATA B).

17. Repeat steps 13 through 14 to check the functionality of the second half of the probe. The acquired data in the State Display menu should resemble the following data when you connect the data signal to J1:

```
0000 A0
                0000 A0
0000 A0
                0000 A0
```

After completing the checks, return the clock jumpers to their original positions and replace the cover on the probe.

Operating Basics

This chapter provides basic operating information for the P6467 High Speed Probe Adapter. The following information is included in this chapter:

- Probe operation
- Descriptions and locations of connectors
- Descriptions and locations of jumpers

Probe Operation

There are two basic operating modes for the P6467 probe that you can set by jumpers J2 and J3, NORM and DIV2. The following sections describe the operating modes and the clock distribution.

NORM Operating Mode

The NORM operating mode lets you acquire data synchronously and asynchronously at speeds up to 100 MHz. The NORM mode acquires data in a similar matter as the standard 92A96 probes. The main difference is that the P6467 probe does not have individual podlet connectors. A 30-pin connector is used to connect to a mating connector on the system-under-test. You can connect the flex cables to one of two mating connectors available from AMP Inc. The two connectors and the pinout information is described in *Appendix A: P6467 High-Speed Probe Adapter Input Connector.*

When you use the probe in the NORM operating mode, the flex cable defined as the Master Clock channel passes the signals from the probe to J200 (bottom two connectors). Jumper J1 (MSTR CLK/EXT) must be in the MSTR CLK position.

You only need to connect one of the probe cables to either of the top two or bottom two probe cable connectors.

DIV2 Operating Mode

The DIV2 mode (divide-by-two) operating mode lets you acquire synchronous data at speeds greater than 100 MHz. If you choose to use the probe in the DIV2 mode, you must be aware of the following limitations of this operating mode:

- Only synchronous acquisitions are allowed.
- You can only use one clock signal with no clock or data qualifications.
- Data is sampled only on the rising edge of the supplied clock.

If you use the DIV2 mode, your logic analyzer must have two 92A96 Modules. Each module must contain one, two, or three 92A96 acquisition cards. One of the 92A96 Module samples data on the rising edge of the clock while the other samples data on the falling edge of the clock.

You must connect two probe cables to each of the J100 and J200 connectors on the P6467 probe. Each pair of probe cables must connect to the same relative position and color-coded connector of each 92A96 Module.

You must also define which P6467 probe acquires the Master clock signal. The flex cable assembly connecting to J400 of that probe is defined as the Master Clock channel and acquires the clock signal.

You can only acquire one clock signal in the DIV2 operating mode. This clock signal is distributed to each of the acquisition cards in the module. If your application requires three-card modules, you must use a clock distribution cable to connect from the Master Clock probe to a second P6467 probe as shown in Figure 3 on page 5. The second P6467 probe provides the clock for the last acquisition card in the module.

In addition to the hardware and clocking requirements, the following setup requirements exist:

- Both modules need to be set to the same trigger program and assert a signal that the other module monitors. (See Figure 8 on page 11 for an example of a sample trigger program.)
- The Clock menu setup requires that each module uses the same clock with one module sampling data on the rising edge of the clock while the other module samples data on the falling edge of the clock.

Clock Distribution

When you use the clock from the Master Clock channel, the clock distribution is essentially the same in the NORM and DIV2 operating modes.

For single-card modules, you must place the MSTR CLK/EXT jumper in the MSTR CLK position. When the jumper is in the MSTR CLK position, the clock drivers connect the Master clock to the probe cables connected to J200.

For two-card modules, you must place the CLK A/MSTR CLK jumper in the MSTR CLK position.

For three-card modules, you must use two P6467 Probes to properly distribute the clock signal on the probe. Place the CLK A/MSTR CLK jumper in the MSTR CLK position on the Master Clock probe. Use one of the external clock connectors, J9 or J10, to drive a second P6467 Probe. Connect a clock cable from J9 or J10 of the Master Clock probe to the EXT CLK IN connector on the second P6467 Probe. You must also place the MSTR CLK/EXT jumper of the second probe in the EXT position.

Transferring Data to the Host

The P6467 Probe acquires data from two acquisition modules on alternate clock edges. In many cases the resultant data may be difficult to use and interpret. The P6467 Probe comes with support software to transfer the acquired data to a host computer and to save the data in a manner that is easier to analyze. You can work with the acquired data directly with host computer applications, or you can save the data in a reference memory for use with the logic analyzer.

Use the CARDATA command to transfer the acquired data to a host computer for use with host computer applications. Use the CARSTORE command to save the acquired data in a reference memory. Both these commands and examples of their use are describe in the *Reference* chapter beginning on page 25.

Figure 10 shows an example of acquired data before using the application software to make the data more readable. Figure 11 shows the same data aligned and saved in a reference memory after executing the CARSTORE command on the host computer.

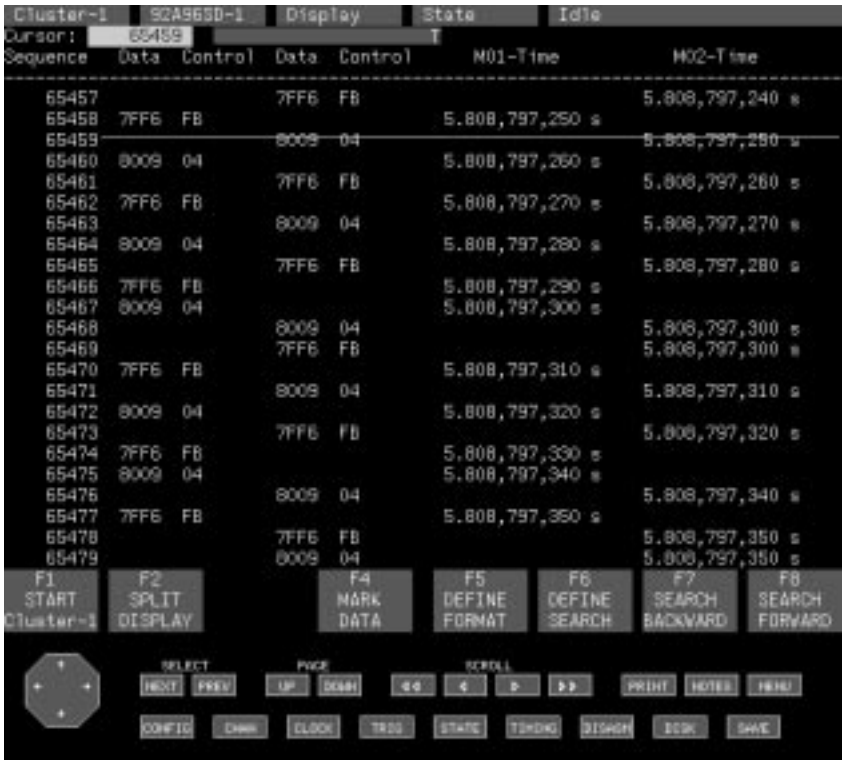


Figure 10: Acquired Raw Data

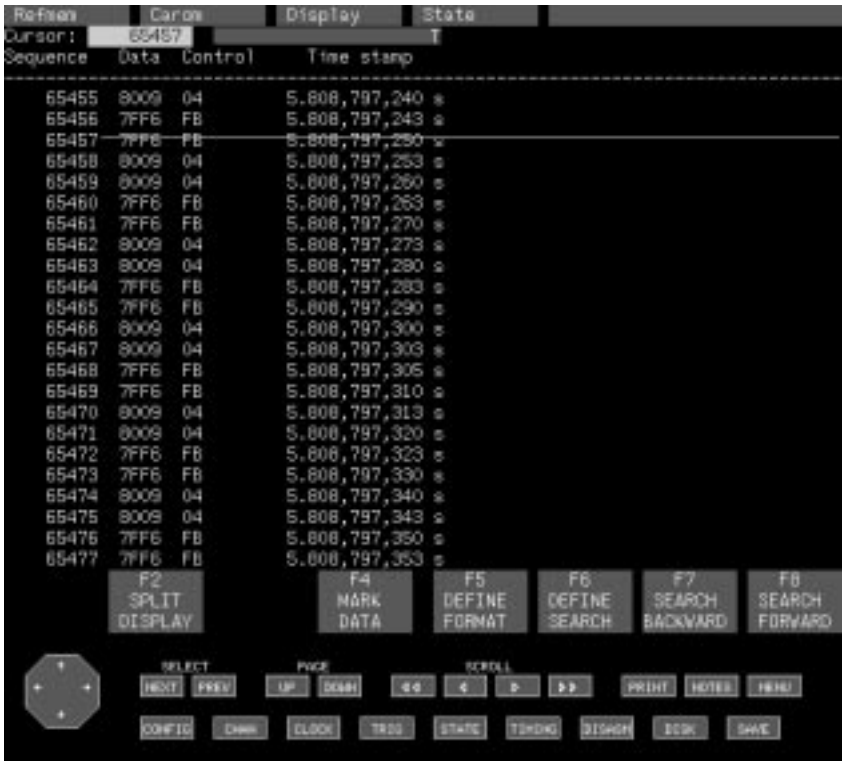


Figure 11: Saved Data from Figure 10.

Descriptions and Locations of Connectors

The P6467 Probe acquires data from a system-under-test and sends the data to the logic analyzer. One probe can aquire data from two 92A96 probe cables from two acquisition modules (one module pair). Figure 12 shows the connectors on the probe (probe covers removed).

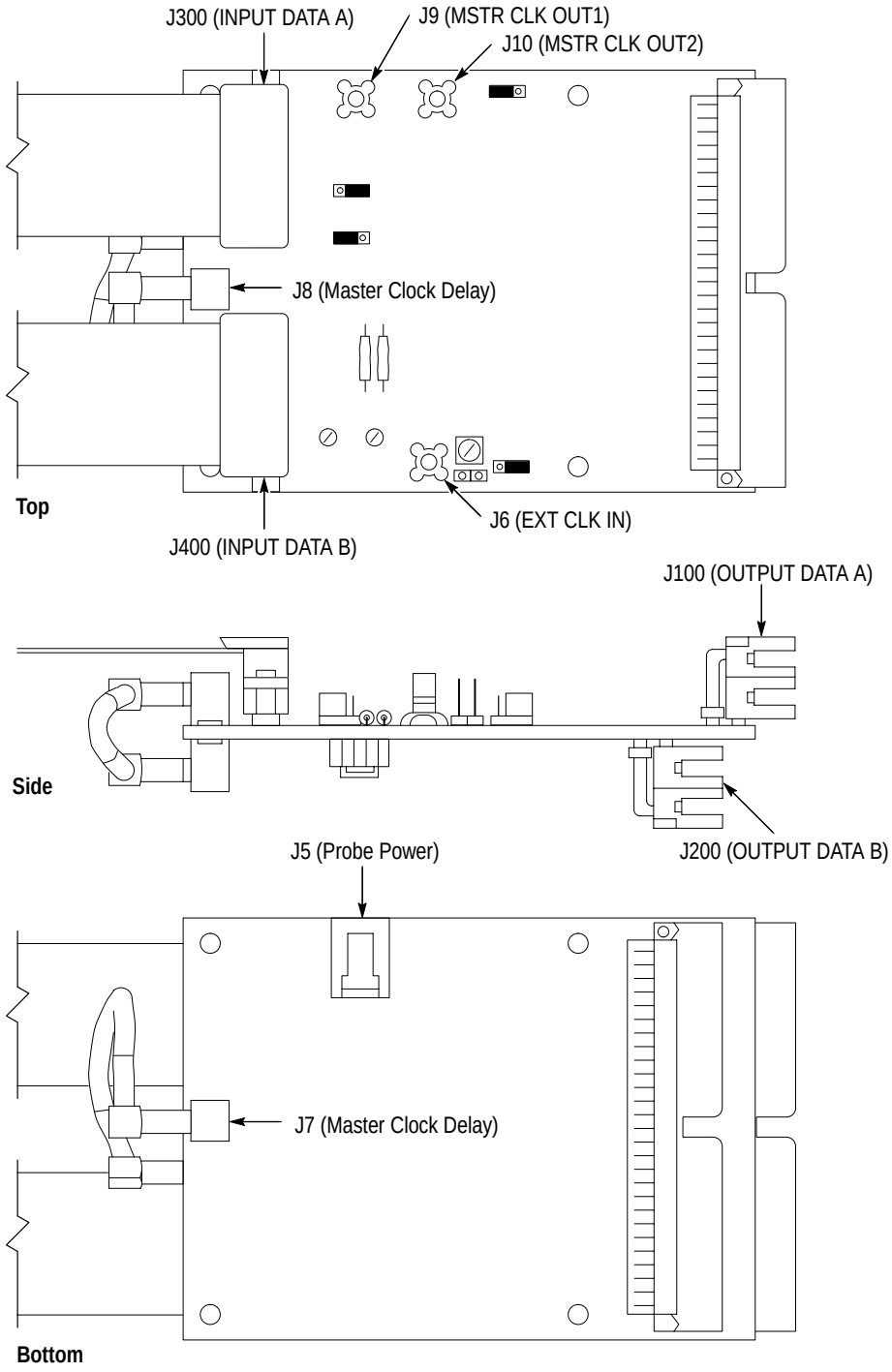


Figure 12: P6467 Probe Connectors

The purpose of each connector on the probe follows:

- J6 (EXT CLK IN). Use this clock input connector when you derive the clock from another P6467 Probe that has been defined as the master clock.
- J7, J8 (MASTER CLOCK DELAY). Use these two connectors to delay the clock transition with longer lengths of 75 Ω cables relative to the data signal transitions (if needed) to meet the setup and hold timing requirements for the logic analyzer.
- J9 (MSTR CLK OUT1), J10 (MSTR CLK OUT2). Use these two connectors if your logic analyzer module needs more than two acquisition cards. These connectors distribute the clock to other P6467 Probes while preserving the timing relationship between the master clock and data on other probes. Use only the clock cable that came with your probe, otherwise the timing relationship can not be guaranteed.
- J300 (INPUT DATA A). This connector is the Data A clock and data input flex connector. The flex cable directs the signals from the system-under-test to the J100 Output Data connector (top two probe connectors) The clock signal from this connector is designated as the CLK A signal at J3.
- J400 (INPUT DATA B). This connector is the Master clock and data input flex connector. This flex cable assembly is designated as the Master clock input for the probe; only the clock input on this flex cable can be designated as the Master clock. The flex cable directs the signals from the system-under-test to the J200 Output Data connector (bottom two probe connectors).
- J100 (OUTPUT DATA A). This connector is the Data A clock and data output connector. The top two 50-pin connectors connect to the 92A96 ribbon or coaxial cable connectors.
- J200 (OUTPUT DATA B). This connector is the Master clock and data channel output connector. The bottom two 50-pin connectors connect to the 92A96 ribbon or coaxial cable connectors.
- J5 (Probe Power). The probe power cable connects to the probe at J5. The probe receives its power from the power connector of the acquisition module in the logic analyzer.

Descriptions and Locations of Jumpers

Figure 13 shows the locations of the jumpers on the P6467 probe. The jumper positions determine the operating mode and clocking of the probe. The probe defined as the Master Clock probe must have the jumpers in the correct positions to operate correctly; the jumper positions have no impact on probes not acquiring clock signals.

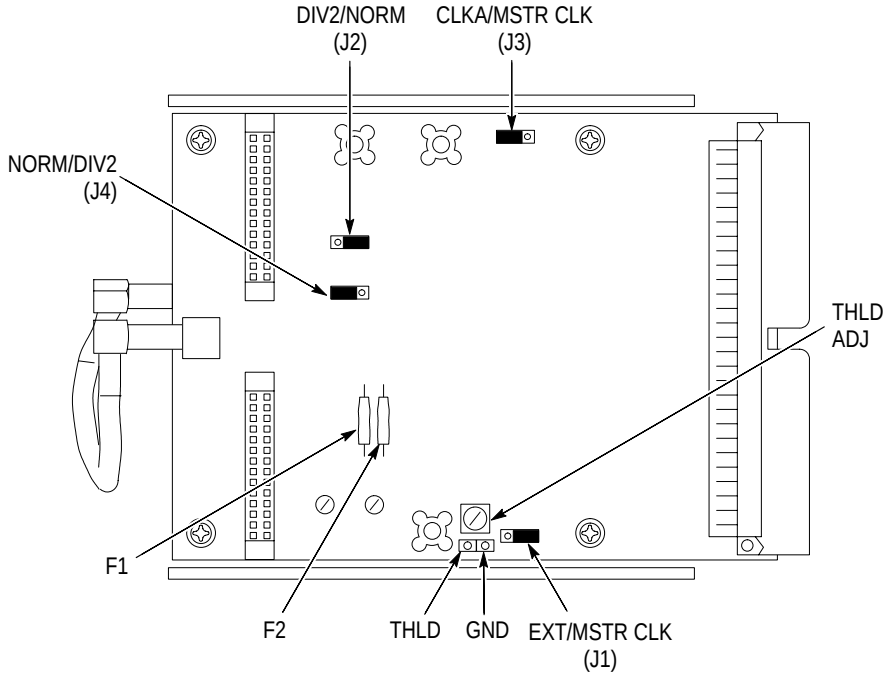


Figure 13: P6467 Clock Jumpers and Clock Threshold Adjustment Locations

A description of each clock jumper follows:

- J1 (MSTR CLK / EXT). This jumper connects either the Clock B Master clock or an external clock from another P6467 probe to the 92A96 probe cables connected to J200 (bottom two connectors) on the probe.
- J2, J3 (NORM/DIV2). These two jumpers determine the operating mode of the probe. Both jumpers *must* be in the same position. The NORM position connects the input Master clock directly to the output drivers. The DIV2 position divides the clock frequency by two before sending the clock signal to the output dividers.
- J4 (CLK A/MSTR CLK). This jumper selects the clock source for the 92A96 probe cables connected to J100 (top two connectors) on the probe.

Use the Clock Threshold Adjustment (THLD ADJ) to set the threshold for the clock inputs. Connect a digital voltmeter to test point THLD and ground and adjust the THLD ADJ control for the desired threshold voltage. Figure 13 shows the location of the THLD ADJ control and the THLD test point.

Reference

This chapter contains information for using the P6467 support software with the High-Speed Probe Adapter with host computer applications. You will find the following information in this chapter:

- P6467 acquisition data commands
- P6467 reference memory commands
- LA-OffLine application examples

The P6467 support software consists of commands to transfer acquired data to a host and to create reference memories. This chapter does not include an exhaustive list of commands and information about using the acquired data with host computer applications. Nor does this chapter provide information on the structure of acquired data files. For information on the content and structure of acquisition data files, refer to the *DAS 9200 Acquisition & Pattern Generation Files User Manual.*

To use the commands in this chapter, you must use the EXEC? Programmatic Command Language (PCL) command with the logic analyzer using either the 92LANP application software or GPIB. For information on using the EXEC? command and other related commands, refer to the *DAS 9200 Programmatic Command Language User Manual*. You should also refer to that manual for a description of the PCL command syntax.

The commands in this chapter follow the PCL command syntax. Refer to the *DAS 9200 Acquisition & Pattern Generation Files User Manual* for details on the command syntax. Some of the more common syntax usage follow:

- Information enclosed by square brackets ([]) is optional.
- Information enclosed by angle brackets (<>) must be supplied by you.
- Arguments for the EXEC? query must be enclosed by single or double quotes.

The following example shows how to use the CARDATA command with the EXEC? query. All the commands described in this section should be used with the EXEC? query in a similar manner.

```
exec? "cardata 92C96-1 92C96-2"
```

P6467 Acquisition Data Commands

The CARDATA command transfers acquired data or information about the data to a host. Several variations of the command are described in the following paragraphs.

Send Acquired Data to the Host

To send acquired data to a host use the CARDATA command with the following syntax:

```
cardata <moduleA> <moduleB> [<first sequence>[<count>[<field>]]]
```

The <moduleA> and <moduleB> arguments define the pair of 92A96 Modules containing the acquired data. The <first sequence> argument specifies the first data sequence to return (the default sequence number is 0). The <count> argument is an integer that specifies the total number of data sequences to return (the default value is 0 for all sequences). Specifying a count of 0 returns all data starting with the <first sequence> and ending at the last data record. The <field> argument specifies the 92A96 data field to return (the default value is 0 for all fields). Table 4 lists the valid 92A96 fields.

Table 4: 92A96 Fields

Field	Description
0	All fields
1	Data fields
3	Timestamps
15	User specfic[1]

1 **For information using field 15, refer to the Tektronix Application Note number 57W-7194-1. Contact your local Tektronix representative for information on obtaining application notes.**

Data records returned by the command are in the same format as the data records returned by the PCL ACQDATA? query.

The following example transfers 500 sequences of acquired data to the host and redirects the data into the file test1. The example uses the 92LANP pclconnect software that supports file redirection (refer to the *92LANP Instruction Manual* for details on using the pclconect software).

```
exec? "cardata ModuleA ModuleB 00 500 0" > test1
```

Reporting the Amount of Data to Return

Use the CARDATA command with the –r switch to report how much data can be returned.

```
cardata –r <moduleA> <moduleB>
```

The <moduleA> and <moduleB> arguments define the pair of 92A96 Modules containing the acquired data. The response to the query is a text string separated commas indicating the first sequence number, sequence count, and the trigger position.

Returning the Acquisition Header Information Only

Use the CARDATA command with the –h switch to return the acquisition data header that is a combination of the headers of both modules. When you use the –h switch, the command returns only the header information.

```
cardata –h <moduleA> <moduleB>
```

The <moduleA> and <moduleB> arguments define the pair of 92A96 Modules containing the acquired data. The channel name information is taken from <moduleA>. The acquisition memory depth is the total number of correlated sequences. The data format of the header is identical to the header returned by the PCL ACQHDR? query.

Returning the Acquisition Header and Data

By default the CARDATA command returns acquired data only. There may be times when you want to return both the header and data information. In this case you can use the CARDATA command with –hd switch.

```
cardata –hd <moduleA> <moduleB>
```

Returning Data Without Timestamp Adjustments

The CARDATA command returns timestamp information. While executing the CARDATA command, there may be duplicate timestamp values. To keep the timestamp values unique, the CARDATA command adjusts the timestamp values by adding 3 ns to the first duplicate timestamp value, 5 ns to the second duplicate timestamp value, and 8 ns to the third duplicate timestamp value. The timestamp corrections are determined for each data record.

Use the optional –t switch with the CARDATA command if you do not want to adjust the timestamp values. If you use the –t switch, duplicate timestamp values can appear in the resultant output.

```
cardata –t <moduleA> <moduleB>
```

The –t switch can be helpful while debugging code for the system-under-test.

P6467 Reference Memory Commands

The CARSTORE command is similar to the MSTORE PCL command. The command provides the additional ability to correlate the data as it is saved.

The CARSTORE command creates a reference memory that contains all of the data in a set of modules that are clustered and correlated. The cluster will include module1 through moduleN as members. Module pairs will be combined and stored as a single module data source. If the cluster contains other correlated data streams not listed on the command line, the data streams will be saved as standard data streams.

The CARSTORE command has the following syntax:

```
carstore [-t] <refmem name> <moduleA> <moduleB> [ -m <moduleA-n2>
<moduleB-n2> [. . . ]]
```

The optional –t switch turns off timestamp corrections. The –t switch works similar to the –t switch in the CARDATA command.

The <refmem name> argument specifies the name of the reference memory to be created. This reference memory will be placed in the Reference_Mem directory on the hard disk of the logic analyzer. You can display the reference memory in the State or Timing display menus.

The <moduleA> and <moduleB> arguments specify a pair of 92A96 Modules. The data from these modules will be combined as the reference memory is saved.

The –m <moduleA-n2> <moduleB-n2> are additional 92A96 Module pairs that will be combined and saved as unique data streams. All modules must be clustered and correlated with <moduleA>. You can only use each module once.

You can also use the –t switch to turn off timestamp adjustments in the reference memory. However, you should avoid using the –t switch when you create a reference memory for more than one pair of 92A96 Modules. Doing so can cause inconsistent results when you display the data in the State menu.

LA–OffLine Applications

If you have the LA-OffLine application installed on the host, you can also view the acquired data of a host file after executing the CARDATA command. Use the following steps to view acquired data with the LA-OffLine application.

1. Use the CARDATA command to transfer data from the logic analyzer to a host file. Use the –hd switch to create a file containing the header and data components of the acquired data.
2. Remove the PCL command header and file-transfer format information from the file to return the file to its raw data form.
3. Convert the raw data file to a LA-OffLine file using the CONVERT command available with the LA-OffLine application.

The following example shows how to transfer data from a logic analyzer using the 92LANP application software. All of commands shown in this example are available with the 92LANP and LA-OffLine application software packages.

1. Use the PCLSEND command to send the acquired data from the logic analyzer named Alpha to the host file test1.

   ```
   pclsend Alpha "exec? 'cardata -hd moduleA moduleB'" > test1
   ```

2. Use the PCLSTRIP command to remove the PCL command header and file-transfer format information.

   ```
   pclstrip test1
   ```

3. Convert the raw data file to a LA-OffLine file named acq.tst1.

   ```
   convert test1 acq.tst1
   ```

4. Delete the raw data file.

   ```
   rm test1
   ```

Specifications

This chapter contains the complete specifications for the P6467 High-Speed Acquisition Probe. Within each section the specifications are arranged in the following functional groups: *Signal Acquisition System, Power Distribution System, Environmental, and Mechanical*.

All specifications are warranted unless they are designated *typical*. Warranted characteristics are checked by procedures in the *Performance Verification* chapter beginning on page 37 ; these characteristics are listed in **boldface** under the Characteristics column.

If the characteristic is noted as *typical*, the characteristic is not warranted. Typical characteristics describe typical or average performance and provide useful reference information.

Table 5: Signal Acquisition System

Characteristic	Description
Number of Input Channels	24 Data, one Clock
Clock Input	
Maximum Clock Frequency	195 MHz, DIV2 Mode 100 MHz NORM Mode
Maximum Differential Input Voltage, typical	3.7 V_{P-P}
Maximum Input Common Mode Voltage Range, typical	–2.0 V to +3.0 V
Minimum Input Voltage Swing	800 mV_{P-P}
Input Load, typical	≤ 6 pF Input Capacitance
Clock Input Threshold Adjustment Range	–1.6 V to +2.6 V
Data Input	
Maximum Data Frequency	97.5 MHz, DIV2 Mode 50 MHz NORM Mode
Input Voltage Levels	
Vin High	+2.0 V Minimum
Vin Low	+0.8 V Maximum
Input Load, typical	≤ 8 pF Input Capacitance

Table 5: Signal Acquisition System (Cont.)

Characteristic	Description
Data Setup Time	2 ns with coaxial probe cables 2.3 ns with ribbon probe cables
Data Hold Time	1.9 ns with coaxial probe cables 2.2 ns with ribbon probe cables

Table 6: Power Distribution System

Characteristic	Description
Power Consumption	< 9 W
External DC Power Source	
Connector Type	Tektronix Part Number 131-5254-XX
Source Voltage	
Connector Pin 1	–15 V to –20 V at < 0.4 A
Connector Pin 2	Ground
Connector Pin 3	+4.75 V to + 5.25 V at < 0.5 A

Table 7: Environmental

Characteristic	Description
Atmospherics	
Temperature	Class 7 Limits except as noted
Operating	+10° C to +50° C
Nonoperating	–55° C to +75° C
Humidity	Class 7 Limits
Operating	+30° C to +40° C, 70% to 75% Relative Humidity
Nonoperating	+30° C to +60° C, 90% to 95% Relative Humidity
Dynamics	
Mechanical Shock	Class 7 Limits
Operating and Nonoperating	Half sine, 100 g, 11 ms duration, three axis, three drops each axis

Table 8: Mechanical

Characteristic	Description
Weight	
Standalone Probe	0.25 kg (0.56 lbs)
Packaged for Domestic Shipment	1.47 kg (3.25 lbs)
Physical Dimensions	
Height	43 mm (1.7 in)
Width	88 mm (3.45 in)
Depth	274 mm (10.8 in), includes flex cables
Cooling Method	Convection
Construction Material	Aluminum Covers

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Performance Verification

This chapter provides performance verification procedures for the P6467 High-Speed Acquisition Probe. It does not include verification procedures for the 92A96 or 92C96 Data Acquisition Modules. Refer to the system service manuals for the DAS or the TLA 500 series logic analyzer for performance verification procedures of the 92A96 and 92C96 Modules.

The functional check procedures are included in the *Getting Started* chapter beginning on page 12. Use the functional check to verify the basic operation of the P6467 Probe.

The following performance specifications are included in this chapter:

- Maximum Clock Frequency
- Minimum Input Voltage Swing
- Clock Input Threshold Adjustment Range
- Input Voltage Levels (Vin High and Vin Low)
- Data Setup and Hold Time

Equipment Required

You will need the following test equipment to complete the performance verification checks in this chapter:

- A TLA 520 Logic Analyzer, DAS/NT, or DAS/XP Logic Analyzer with two 92A96 or 92C96 Data Acquisition Modules
- One or more P6467 High-Speed Probe Adapters with a Probe Power cable
- One Tektronix HFS 9003 Stimulus System with one HFS 9DG1 Data Generator and two HFS 9DG2 Data Generators
- Two sets of coaxial probe cables (Tektronix part number 198-5761-XX) or two sets of standard 92A96 probe cables
- One Digital Voltmeter, 3.5 digit with 0.1% accuracy
- One P6467 Test Fixture (Tektronix part number 067-0262-XX)
- Thirteen 20-inch long 3 mm coaxial cables (Tektronix part number 174-1427-XX)

- Oscilloscope with FET probes with bandwidth sufficient to measure relative time delays of approximately 5 ns
- 50 Ω Termination (Tektronix part number 011-0049-01)
- One 42-inch 50 Ω coaxial cable (Tektronix part number 012-0057-01)

Performance Verification Procedure

Before attempting any of the procedures in this section, allow a minimum of a 20 minutes to warm up all test equipment. These instructions assume that you perform the performance verification check while abiding by the environmental conditions as described in Table 7 on page 32.

The following procedures are designed to test one P6467 Probe at a time. Repeat the procedures for each additional probe.

Test Equipment Setups

The following steps describe the test equipment setups for the logic analyzer and for the HFS 9003 Stimulus System. These steps assume that your DAS or TLA logic analyzer already have the 92A96 Modules installed and that the Probe Cables are properly connected to the 92A96 Modules. These steps also assume that you have installed the P6467 Application Support software on the logic analyzer.

Logic Analyzer Setups. The following steps describe how to connect the probes to the logic analyzer and how to set up the logic analyzer menus for the performance verification checks.

NOTE*. The following procedures assume that the 92A96 Modules are located in slots two and three of the logic analyzer. If your logic analyzer has the 92A96 Modules in different slots, you must adjust these procedures accordingly.*

1. Remove the cover from each P6467 Probe that you are testing and set the cover aside.
2. Connect the probe power cable from one of the 92A96 Modules in the logic analyzer to the power connector on the P6467 Probe (if necessary, refer to Figure 5 on page 7 for connection information). Leave the unused end of the probe power cable disconnected.
3. Connect the blue-labeled coaxial probes from the logic analyzer to the OUTPUT DATA A Connector (top or J100) of the P6467 Probe.
4. Power on the logic analyzer and wait for the Menu Selection overlay to display.

NOTE. *The P6467 Application Support software includes a predefined setup that you can restore and use with the following setups. To use the predefined setups, select the Save/Restore menu and restore the setup file named P6467_PVD. Otherwise continue with the following steps to manually set up the logic analyzer.*

5. Select the **Sys Config** menu and perform the following steps:
   - **a.** Select a Module formation with two individual 92A96 Modules.
   - **b.** Change the module names to **module_a** (module_a should be the 92A96 module in the lowest numbered slot in the logic analyzer) and **module_b**.
   - **c.** Select **F6: DEFINE CLUSTER** and define a cluster named P6467 containing the two 92A96 Modules.
6. Select the **Clus Setup** menu and perform the following steps:
   - **a.** Select **F4 DEFINE CORRELATN** and correlate the two 92A96 Modules (select **module_a** in the Correlate field, select **F7: ADD COR**, select **module_b** in the new field, and save the changes).
   - **b.** Select **F2: DEFINE SIGNAL** and select **F7: ADD SIGNAL**.
   - **c.** Define a signal **AtoB** with the module_a Direction field set to **Output** and the module_b Direction field set to **Input**.
   - **d.** Select **F7: ADD SIGNAL** and define a second signal **BtoA**.
   - **e.** Set the module_a Direction field to **Input** and the module_b Direction field to **Output**.
   - **f.** Save and close the overlay and verify that the Clus Setup menu displays the signal definitions.
7. Select the module_A Config menu and set the Acquisition Memory field to **32768** cycles.
8. Select the Channel menu and perform the following steps:
   - **a.** Select F5: DEFINE THRESHOLD to call the Threshold Definition overlay.
   - **b.** Change the Clock Threshold field to **VAR –1.85 V**.
   - **c.** Change the Data Threshold field to **VAR +1.95 V**.
   - **d.** Save the changes and close the overlay.
   - **e.** Delete the Address group from the Channel menu.

f. Delete Sections D3 and D2 from the Data group.

g. Delete Sections C3, C1, and C0 from the Control group.

h. Ensure that the Input Radix is set to **Hex** for the remaining groups.

9. Select the Clock menu and perform the following steps:

a. Change the Clock field to **External**.

b. Select the rising edge of Clock_2 with no qualification.

10. Select the Trigger menu change it to match Figure 14.

Figure 14: Trigger Menu Setup

11. Repeat steps 7 through 10 for the module_b setups with the following exceptions:

a. In the Clock menu, select the falling edge of Clock_2 instead of the rising edge.

b. In the Trigger menu, assert Signal **BtoA** instead of Signal **AtoB,** and change the last event to monitor Signal **AtoB** instead of Signal **BtoA**.

HFS 9003 Stimulus System Setups. The following steps describe how to set up the menus for the HFS 9003 Stimulus System for the performance verification procedures.

NOTE. *The followings steps use a HFS 9003 Stimulus System with an HFS DG1 module in slot C (top) and two HFS DG2 modules in slots B and A (middle and bottom slots). If your HFS 9003 Stimulus System has the modules in a different arrangement, the slot identifiers for the modules in Table 9 will differ.*

1. Connect the 20-inch, 3 mm coaxial cables to the following outputs of the HFS 9003 Stimulus System modules: A1, A2, A3, A4, B1, B2, B3, B4, C1, C3, $\overline{C3}$, C4, and $\overline{C4}$.
2. Perform a skew cal for each of the data signals by connecting the end of each cable to the SKEW CAL IN connector (if necessary, refer to HFS 9003 Stimulus System documentation for information on running the skew cal).
3. Refer to Table 9 and enter the setups for the HFS 9003 Stimulus System. Be aware that you must set the characteristics of each individual data channel (setting the characteristics of one data channel does *not* automatically set the characteristics of the remaining data channels).

Table 9: HFS 9003 Stimulus System Menu Setups

	HFS DG1 Clock Channel	**HFS DG2 Data Channels**		**HFS DG1 Data Channels**
	C1	**A1, A3, B1, B3**	**A2, A4, B2, B4**	**C3, $\overline{C3}$, C4, $\overline{C4}$**
High Level	+2.4 V	+2 V	+2 V	+2 V
Low Level	+1.6 V	+800 mV	+800 mV	+800 mV
Polarity	Normal	Normal	Complement	Normal
Frequency	20 MHz	20 MHz	20 MHz	20 MHz
Lead Delay	3 ns	5 ns	5 ns	5 ns
Duty Cycle	50 %	50 %	50 %	50 %
Transition	200 ps	800 ps	800 ps	200 ps
Pulse Rate	Norm	Quarter	Quarter	Quarter
Output	On	On	On	Output On, $\overline{\text{Output On}}$
Signal Type	Pulse	Pulse	Pulse	Pulse

4. If desired, save the test setups of HFS 9003 Stimulus System; refer to your HFS 9003 user documentation for information on saving setups.

5. Connect the data generator outputs to the inputs of the P6467 Test Board in the following manner:

   a. Connect the clock signal C1 to J13 on the test board.

   b. Refer to Table 10 and connect the outputs of the two HFS DG2 generators to the connections at J1 through J8 on the test board.

   c. Refer to Table 10 and connect the number 3 and 4 outputs of the HFS DG1 to the connections J9 through J12.

Table 10: HFS 9003 Stimulus System to P6467 Test Board Connections

HFS 9003 Stimulus System	P6467 Test Board
A1	J1
A2	J2
A3	J3
A4	J4
B1	J5
B2	J6
B3	J7
B4	J8
C3	J9
$\overline{C3}$	J10
C4	J11
$\overline{C4}$	J12
C1	J13

Final Deskew Setups. In certain situations, such as when setting up new test equipment or after recalibrating the HFS 90003 Stimulus System, you need to use an oscilloscope to perform the final deskew setups before performing the procedures in this section.

1. Connect the 42-inch 50 Ω coaxial cable from the HFS 9003 Trigger Out to the external trigger input of the oscilloscope through the 50 Ω termination.

2. Set up the oscilloscope to trigger externally from the HFS 9003 Stimulus System. Set the oscilloscope time base to 0.5 ns/DIV and the volts/Division to 0.2 V/DIV.

3. Connect the FET probe to the clock signal (pin 2) and one of the ground pins of J100 on the P6467 Test Board.

4. Adjust the oscilloscope to establish a common reference point for the clock signal. For example, adjust the display so that the threshold level (50% point of the signal) is at the center of the display. Move the Horizontal Position control to move the rising edge of the clock signal 2 ns to the left of the center graticule.

5. Move the FET probe to one of the data signals of J100 on the P6467 Test Board (if necessary refer to Table 15 on page 64 for the identification of the data signals at J100). Note where the data transition occurs with respect to the reference point of the rising edge of the clock signal.

6. Check that the data signal is at the center of the display (2 ns after the rising edge of the clock). If not, adjust the lead delay of the selected clock signal on the HFS 9003 Stimulus System to set the 50% point of the data signal to the center of the display (2 ns from the clock edge).

7. Repeat step 6 for each data signal.

This completes the test equipment setup.

Clock Threshold Adjustment Range Check

This check verifies the Clock Threshold Adjustment Range (–1.6 V to +2.6 V). Perform the following steps to verify the specification:

1. Connect the positive lead of the digital voltmeter to test point THLD on the probe; connect the negative lead to the ground test point adjacent to THLD (if necessary refer to Figure 4 on page 6 or to Figure 13 on page 23 for the test point location).

2. Rotate the threshold adjustment control (THLD ADJ) through the full range and note the reading on the voltmeter.

3. Check that you can vary the threshold voltage from –1.6 V to +2.6 V.

4. Set the threshold voltage to +2.0 V (± 10 mV) and disconnect the voltmeter leads.

Setup & Hold Timing and Maximum Operating Frequency Check

This check verifies the Setup & Hold timing for the P6467 Probe and concurrently verifies the clock maximum operating frequency, the minimum input voltage swing, and the input voltage levels. An overview of the check appears at the end of these instructions. The tests are designed to use one of the flexible leads of the P6467 Probe at a time.

1. If you have not already done so, refer to Table 9 and enter the setups for the HFS 9003 Stimulus System.

2. Set the jumpers on the P6467 Probe to the positions listed in Table 11.

Table 11: Jumper Positions for the Setup & Hold and Maximum Operating Frequency Check

P6467 Probe Jumper	Jumper Position
J1 (EXT/MSTR CLK)	MSTR CLK
J2 (NORM/DIV2)	NORM
J3 (CLK A/MSTR CLK)	CLK A
J4 (DIV2/NORM)	NORM

3. Connect the INPUT DATA A flex cable of the probe to the P6467 Test Fixture.

4. On the logic analyzer, select the State Display menu and select **F1: START** to start the check.

***NOTE**. If the logic analyzer displays a SLOW CLOCK message, check that all of the jumpers are in the correct positions on the probe and that you have correctly connected the clock signal from the HFS 9003 Stimulus System to the P6467 Test Board.*

5. Check that the logic analyzer does not trigger and displays the Monitor menu. Check that Counter #1 runs and increases in value.

***NOTE**. If a line transient or if stray electrical noise causes the logic analyzer to trigger, repeat the test at least three times and verify that the the logic analyzer does not stop and trigger at the same time for each test.*

If the logic analyzer triggers and displays the incorrect data, verify that you have the correct setups for the HFS 9003 Stimulus System and that you have defined the setups for all the data channels.

6. Wait for Counter #1 to run for at least ten seconds and verify that the logic analyzer does not trigger; then select **F1: STOP**.

7. Check that the State Display menu looks similar to the following repeating data sequence:

```
AAAA AA
              5555 55
AAAA AA
              5555 55
5555 55
              AAAA AA
5555 55
              AAAA AA
AAAA AA
              5555 55
```

If the P6467 Probe acquires incorrect data, the logic analyzer will trigger and display the faulty data.

***NOTE**. If you restored the logic analyzer setups from the setup file on the hard disk, the display will show timestamps in addition to the data. The timestamps are not required for these procedures.*

8. Change the HFS 9003 Stimulus System clock channel (C1) LEAD DELAY to 7.0 ns (7.3 ns if you have ribbon probe cables) and repeat steps 4 through 7.

9. Refer to Table 12 and repeat steps 4 through 8 for each test frequency and clock lead delay.

Table 12: Test Setups for the NORM Operating Mode

P6467 Test Board Connection	92A96 Probe Cable Connection	Test Frequency	Clock Lead (C1) Delay	
			Coaxial Cables	Ribbon Cables
INPUT DATA A	OUTPUT DATA A	20 MHz	3.1 ns	2.8 ns
INPUT DATA A	OUTPUT DATA A	20 MHz	7.0 ns	7.3 ns
INPUT DATA A	OUTPUT DATA A	100 MHz	7.0 ns	7.3 ns
INPUT DATA A	OUTPUT DATA A	100 MHz	3.1 ns	2.8 ns
INPUT DATA B	OUTPUT DATA B	100 MHz	3.1 ns	2.8 ns
INPUT DATA B	OUTPUT DATA B	100 MHz	7.0 ns	7.3 ns
INPUT DATA B	OUTPUT DATA B	20 MHz	7.0 ns	7.3 ns
INPUT DATA B	OUTPUT DATA B	20 MHz	3.1 ns	2.8 ns

10. Move jumpers J2 and J4 on the P6467 Probe to the DIV2 positions.

11. Set the HFS 9003 Stimulus System test frequency to 100 MHz.

12. Select **F1: START** for and check that the logic analyzer does not trigger.

13. After ten seconds, select **F1: STOP** and check that the State Display menu looks similar to the following repeating data sequence:

```
AAAA AA
             5555 55
5555 55
             AAAA AA
AAAA AA
             5555 55
5555 55
             AAAA AA
AAAA AA
             5555 55
```

The acquired data for each column should be a repeating sequence as shown; however, the data may not line up between the two columns as shown. A failed test is indicated by wrong data.

14. Repeat steps 12 through 13 for each test frequency and clock lead delay setting in Table 13.

Table 13: Test Setups for the DIV2 Operating Mode

P6467 Test Board Connection	92A96 Probe Cable Connection	Test Frequency	Clock Lead (C1) Delay	
			Coaxial Cables	Ribbon Cables
INPUT DATA B	OUTPUT DATA B	100 MHz	3.1 ns	2.8 ns
INPUT DATA B	OUTPUT DATA B	100 MHz	7.0 ns	7.3 ns
INPUT DATA B	OUTPUT DATA B	165 MHz	7.0 ns	7.3 ns
INPUT DATA B	OUTPUT DATA B	165 MHz	3.1 ns	2.8 ns
INPUT DATA B	OUTPUT DATA B	195 MHz	3.1 ns	2.8 ns
INPUT DATA B	OUTPUT DATA B	195 MHz	7.0 ns	7.3 ns

If you have coaxial probe cables, the Hold time is checked when you set the LEAD DELAY of the data channels to 5 ns and the clock channel LEAD DELAY to 3.1 ns (T_{hold} = 1.9 ns). The Setup time is checked when you set the clock channel LEAD DELAY to 7 ns (T_{setup} = 2 ns).

If you have ribbon probe cables, the Hold time is checked when you set the LEAD DELAY of the data channels to 5 ns and the clock channel LEAD DELAY to 2.8 ns (T_{hold} = 2.2 ns). The Setup time is checked when you set the clock channel LEAD DELAY to 7.3 ns (T_{setup} = 2.3 ns).

The Trigger menu setups are designed such that the logic analyzer will not trigger as long as it acquires the correct data patterns. The data patterns from the HFS 9003 Stimulus System consist of AAAA AA and 5555 55 for each sequence. Start the logic analyzer from the State Display menu. The logic analyzer should not trigger; instead the Monitor menu should appear and display a counter running. The test passes when the counter runs for approximately ten seconds or the counter value exceeds 1,000,000,000. Manually stop the logic analyzer to stop the test.

Clock Distribution Checks

This check verifies the Clock Distribution on the P6467 Probe. Use the same setups for the HFS 9003 Stimulus System listed in Table 9 on page 41 except for the frequency–change the frequency to 100 MHz.

1. Refer to Table 14 and set the P6467 Probe jumpers for each one of the clock configuration setups to verify the proper clock operation.
2. Select **F1: START** and verify that the logic analyzer does not trigger.
3. Select **F1: STOP** and check the acquired data.
4. Repeat steps 2 and 3 for each setup in Table 14.

Table 14: Jumper Positions and Clock Cable Connections

Setup Number	Jumper J1	Jumper J2	Jumper J3	Jumper J4	Clock Distribution Cable Connections from	to
1	MSTR CLK	NORM	NA	NORM	NA	NA
2	EXT	NORM	NA	NORM	MSTR CLK OUT 1	EXT CLK IN
3	EXT	NORM	NA	NORM	MSTR CLK OUT 2	EXT CLK IN
4[1]	NA	NORM	CLK A	NORM	NA	NA
5[2]	NA	NORM	MSTR CLK	NORM	NA	NA

[1] **For this setup, move the blue-labeled probe from OUTPUT DATA B (bottom connector pair) to OUTPUT DATA A (top connector pair). Move the test signal connection to the INPUT DATA A flex cable connector.**

[2] **For this setup, the logic analyzer should trigger and display zeros instead of the A/5 data.**

5. Check that the acquired data in the State Display menu looks similar to the following repeating data sequence:

```
                5555 55
AAAA AA
                5555 55
AAAA AA
                AAAA AA
5555 55
                AAAA AA
5555 55
                5555 55
AAAA AA
```

These checks verify that a clock signal can be distributed to all clock connections on the probe. If any checks fail, verify that all jumpers and connectors are in the correct locations as described in Table 14. Also, verify the correct setups for the HFS 9003 Stimulus System.

If the tests still fail after verifying all of the setups, repair is necessary. Contact your local Tektronix representative for repair and replacement information.

Adjustment Procedures

There are no sevice adjustment procedures required for this product.

Maintenance

This chapter provides procedures and information for inspecting and cleaning the P6467 High-Speed Probe Adapter, removing and replacing probe components, and isolating problems to specific components.

Service Strategy

The basic service strategy is to isolate faults to a module level and replace any faulty modules with good modules. Any modules requiring repair should be returned to your local Tektronix service center.

Performance verification can be accomplished by following the procedures in the *Performance Verification* chapter beginning on page 37. There are no diagnostics available for the P6467 assemblies. However, power-on diagnostics exist for the 92A96 Data Acquisition Modules. Refer to the *DAS 9200 Technician's Reference Manual* for information on the power-on diagnostics for the 92A96 Modules.

Preparation

The information in this chapter is designed for use by qualified service personnel. Read the *Safety Summary* at the front of this manual and the *Service Safety Summary* before attempting any procedures in this chapter. Refer to the *Operating Basics* chapter for information on the location of jumpers and probe connections.

CAUTION. *Components on the P6467 Probe can be damaged by static discharge. Service the probe only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the probe. Always wear a grounded wrist strap, or equivalent, while servicing the probe.*

Observe the following precautions to avoid damaging the probe:

- Do not handle static-sensitive components on the probe.
- Transport and store the probe in its original container or on conductive foam. Label any package that contains static-sensitive assemblies.
- Wear a wrist strap to discharge static electricity from your body.
- Do not allow anything capable of generating or holding a static charge on the work surface.

- Do not slide the probe over any surface.
- Avoid handling the probe in areas that have a floor or work surface cover that is capable of generating a static charge.

CAUTION. *To prevent damage to the probe, always disconnect the probe from the DAS or TLA mainframe and from the system-under-test before servicing or cleaning the probe.*

Inspection and Cleaning

The P6467 Probe is inspected mechanically and electrically before shipment from the factory. The probe should be free of marks or scratches and should meet and exceed all electrical specifications. To confirm this, inspect the probe for physical damage during transit. Save the probe packaging in case shipment or repair is necessary. Contact your local Tektronix representative if there is any damage or deficiency.

Cleaning procedures consist of exterior cleaning only. Periodic cleaning reduces instrument failure and increases reliability. Clean the probe as needed, based on the operating environment.

CAUTION. *Do not use chemical cleaning agents; they may damage the probe. Avoid using chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.*

Clean the exterior surfaces of the probe with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, use a cloth or swab dipped in a 75% isopropyl alcohol solution. Use a swab to clean around controls or connectors. Do not use abrasive compound on any part of the probe.

Removal and Replacement Instructions

The P6467 Probe has a limited number of components that can be replaced. All replaceable parts are listed in the *Replaceable Parts* chapter beginning on page 55. You can access all of components on the probe after removing the top cover. Remove the top cover by removing the two screws on each side of the probe.

Troubleshooting Procedures

Use the following information to isolate problems to the probe or to the logic analyzer. You can monitor any error messages that display on the logic analyzer screen.

Slow Clock. The logic analyzer starts but does not receive a clock from the probe. If this message displays on the logic analyzer, check for one or more of the following possible problems:

- Verify the jumpers on the probes are in the correct positions for your application. If necessary, refer to Figures 1 through 4 on pages 3 through 6 in this manual for the jumper settings and locations.
- Verify that the probe power cable is connected and delivers power to the probe.
- Check the fuses on the P6467 Probe.
- Verify that you have the correct clock selected in the Clock menu for *both* acquisition modules.
- Verify that you have the Trigger menu set up properly for *both* acquisition modules.
- Verify that the flex cables of the probe are correctly connected to the system-under-test.
- Verify the threshold voltage is set properly on the probe.
- Verify that the threshold voltage on *both* Channel menus is set correctly.

Incorrect Data Acquired. If the logic analyzer acquires incorrect data, check for one or more of the following possible problems:

- Verify that the NORM/DIV2 jumpers are in the correct positions on the probe.
- Isolate the problem to a faulty probe by substituting a known good probe (ensure that you place the jumpers in the correct positions if you replace one of the probes that acquires the clock signals.
- Verify the threshold voltage is set properly on the probe.
- Verify that the threshold voltage on *both* Channel menus is set correctly.

Theory of Operation

The P6467 probe acquires data through two flexible leads at J300 and J400. The data flows through a compensation network before being passed on to the 92A96 probe cables at J100 and J200.

In addition to acquiring data at J400, the probe also acquires a master clock signal (B_Clock). The clock signal passes through a delay line at J8 and J7. The cable delays the clock transitions relative to the data transition to meet the setup and hold timing of the logic analyzer. The amount of delay depends on the length of the cable between J7 and J8. The clock signal passes to jumpers J2 and J4 where the user selects the normal mode (NORM) or divide-by-two mode (DIV2). The clock signal is distributed to the probe cables at J100 and J200 depending on the settings of jumpers J3 and J1. You can also use the clock signal to drive other P6467 probes by connecting clock cables at J9 and J10.

The position of jumper J1 (EXT/MSTR CLK) lets you drive the probe cable connected to J200 by the Master clock or by a an external clock signal (from another P6467 probe) connected to J6.

The position of jumper J3 (CLK_A/MSTR CLK) determines the clock signal sent to the probe cable at J100. When the jumper is in the MSTR CLK position, the Master clock is sent to J100. When the jumper is in the CLK_A position. the clock signal (A_Clock) from the flex cable at J300 is sent to the probe cable connected to J100.

For any other P6467 probes that do not acquire any clock signals, the data passes from the flex leads through the probe to the 92A96 probe cables.

Two fuses protect the power supply voltages of the probe. Fuse F1 monitors the +5 V line and Fuse F2 monitors the –15 V input which becomes the –5 V line on the probe. The part numbers of the fuses are listed in *Replaceable Parts*.

Replaceable Parts

This section contains a list of the replaceable modules for the P6467 High–Speed Probe Adapter. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

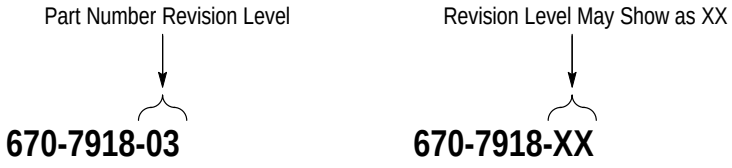
- Part number (see Part Number Revision Level below)
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Part Number Revision Level

Tektronix part numbers contain two digits that show the revision level of the part. For most parts in this manual, you will find the letters XX in place of the revision level number.



When you order parts, Tektronix will provide you with the most current part for your product type, serial number, and modification (if applicable). At the time of your order, Tektronix will determine the part number revision level needed for your product, based on the information you provide.

Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

Module Exchange. In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEK-WIDE, extension 6630.

Module Repair and Return. You may ship your module to us for repair, after which we will return it to you.

New Modules. You may purchase replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the P6467 High–Speed Probe Adapter. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts List Column Descriptions

Column	Column Name	Description
1	Figure & Index Number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix Part Number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial Number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & Description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. Code	This indicates the code of the actual manufacturer of the part.
8	Mfr. Part Number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers Cross Index

Mfr. Code	Manufacturer	Address	City, State, Zip Code
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609–3320
TK0588	UNIVERSAL PRECISION PRODUCTS	1775 NW 216TH	HILLSBORO OR 97123
TK1465	BEAVERTON PARTS MFG CO	1800 NW 216TH AVE	HILLSBORO OR 97124–6629
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY SUITE #2	VANCOUVER WA 98601
TK2547	XEROX CORPORATION HARRISON SQUARE	SUITE 250 1800 SW FIRST STREET	PORTLAND OR 97201
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
0GZV8	HUBER AND SUHNER INC	ONE ALLEN MARTIN DRIVE	EXXEX VT 05451
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661–2999
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR PO BOX 547	FRANKLIN IN 46131
5Y400	TRIAX METAL PRODUCTS INC DIV OF BEAVERTON PARTS MFG CO	1800 NW 216TH AVE	HILLSBORO OR 97124–6629
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
75915	LITTELFUSE TRACOR INC SUB OF TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016–3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
1–0	010–6467–XX			1	PROBE,ACQ:HI–SPEED;P6467	80009	0106467XX
–1	380–1102–XX			1	HOUSING,HALF:UPPER HALF HOUSING,0.063 AL SHEET,ALLOY	5Y400	380–1102–XX
–2	211–0244–XX			8	SCR,ASSEM WSHR:4–40 X 0.312,PNH,STL,CD PL,POZ, MACHINE	TK0435	7772–312
–3	211–0105–XX			4	SCREW,MACHINE:4–40 X 0.188,FLH,100 DEG,STL	TK0435	MACHINE SCREW:
–4	671–3400–XX			1	CKT BD ASSY:TERMINATION;389–2022–XX WIRED,P6467	80009	671340000
–5	131–5829–XX			4	CONN,SHUNT:JUMPER,;FEMALE,STR,1 EA,2MM,4MMH (P1,P2,P3,P4)	00779	382575–3
–6	131–5990–XX			4	CONN,HDR PCB;MALE,STR1 X 36,0.079 CTR,0.146 MLG X 0.118 TAIL,GOLD (J1,J2,J3,J4)	55322	TMM–136–01–G–2
–7	131–1857–XX			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD (TP1,TP2)	58050	082–3644–SS10
–8	131–5989–XX			2	CONN,BOX SMD,;FEMALE,STR,2 X 20,0.05 X 0.1 CTR,0.370 H,GOLD, W/B0ARD RETENTION	55322	TMM–136–02–G–2
–9	131–4955–XX			2	CONN,HDR::PCB,;MALE,RTANG,4 X 25 0.1CTR,0.640 H X 0.155 TAIL,SHRD/4 SIDES,CTR PLZ,30 GOLD,(2)2 X 25,W/O LATCH (J300,J400)	TK1465	131–4955–XX
	131–4634–XX			3	CONN,RF JACK SMD,;50 OHM,MALE,STR,0.325 H X 0.159 TAIL (J6,J9,J10 NOT ILLUSTRATED)	JC011B	221111–1
–10	131–5254–XX			1	CONN,HDR:PCB,;MALE,RTANG,1 X 3,0.1 CTR,0.2 H X 0.13 TAIL,SHRD/4SIDES,LATCHING,TIN (J5)	00779	103672–2
–11	380–1103–XX			1	HOUSING,HALF:LOWER HALF HOUSING,0.063 AL SHEET, ALLOY	5Y400	380–1103–XX
–12	129–0499–XX			4	SPACER,POST:0.72 L,4–40 THRU,AL,0.188 HEX	TK0588	ORDER BY DESC
–13	131–0265–XX			2	CONN,RF JACK:SMB,;PCB,MALE,RTANG,50 OHM,0.381 H X 0.15 TAIL,0.043 DIA CTR COND,0.040 SQ TAIL (J7,J8)	0GZV8	85SMB–50–0–1
–14	174–3126–XX			1	CABLE ASSY,:COAX,;RFD,75 OHM,2.7L,SMB,FEMALE, RTANG,EACH END	TK2469	174–3126–XX
–15	259–0144–XX			2	FLEX CIRCUIT:INTERCONNECT TO PROBE ADAPTERBOARD,CAROM	80009	2590144XX
–16	159–0159–XX			2	FUSE,WIRE LEAD:1.5A,125V,5 SEC, (F1,F2)	75915	25101.5

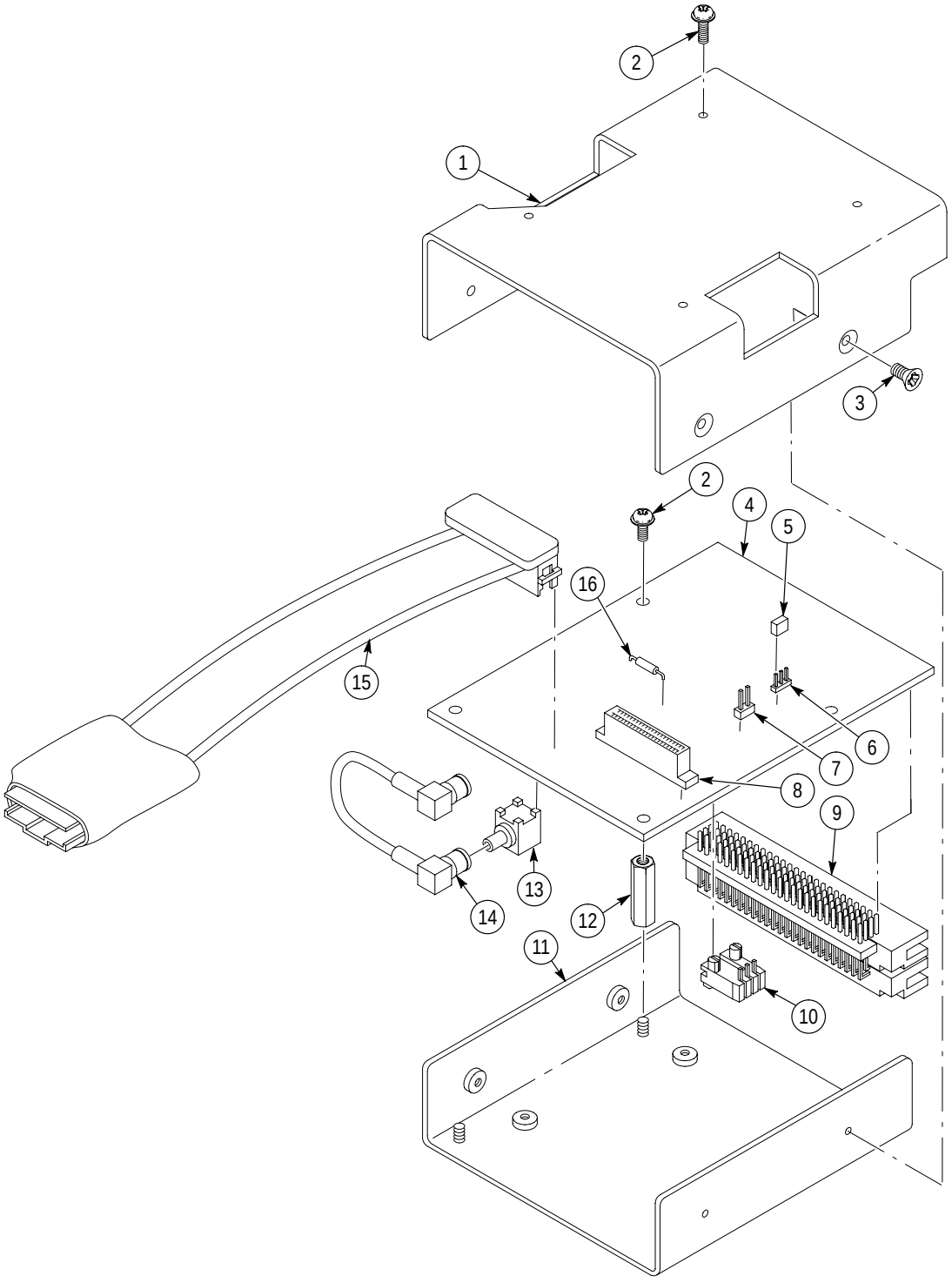


Figure 1: Exploded view

Replaceable Parts List

Fig. & Index Number	Tektronix Part Number	Serial No. Effective	Serial No. Discont'd	Qty	Name & Description	Mfr. Code	Mfr. Part Number
					OPTIONAL ACCESSORIES		
2–0	067–0262–XX			1	FIXTURE,CAL:HI–SPEED PROBE TEST FIXTURE;P6467	80009	0670262XX
–1	211–0658–XX			4	SCR,ASSEM WSHR:6–32 X 0.312,PNH,STL,POZ	TK0435	17691–300
–2	131–0663–XX			13	CONN,RF JACK:SMA,;50 OHM,FEMALE,STR,PCB,0.391 H X 0.150 TAIL,(4) 0.04 SQ TAILS W/0.2 SQ PCB (J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13)	24931	39JR162–1
–3	671–3635–XX			1	CKT BD ASSY:HI–SPEED PROBE TEST FIXTURE	80009	6713635XX
–4	131–6023–XX			1	CONN,BOX:PCB,;FEMALE,STR,2 X 15,0.05 X 0.1 CTR,0.350 X 0.1 TAIL,30 GOLD, SYS 50 (J100)	80009	1316023XX
					STANDARD ACCESSORIES		
–5	174–3506–XX			1	CA ASSY,RF:COAX,;RFD,75 OHM.10.00 L,SMB PLUG, FEMALE,RTANG AT EACH END,FIXED DELAY 1.04NS +/– 0.05NS	TK2469	174–3506–XX
–6	174–3502–XX			1	CA ASSY,SP:DESCRETE,;CPD,4,22 AWG,72.0 L,MINI FIT JR,4 POS(2X2) X (2) 1X3,0.1 CTR,LATCHING	80009	1743502XX
–7	348–0187–XX			4	FOOT,CABINET:BLACK POLYURETHANE, (THIS IS A SUB–PART OF TEST FIXTURE ITEM 3 ABOVE)	0JR05	ORDER BY DESC
	070–9176–XX			1	MANUAL,TECH:INSTRUCTION,P6467,DP	TK2547	070–9176–XX
	070–8364–XX			1	MANUAL,TECH:REFERENCE,DAS9200 92LANP,DP	TK2548	PER TEK P/N

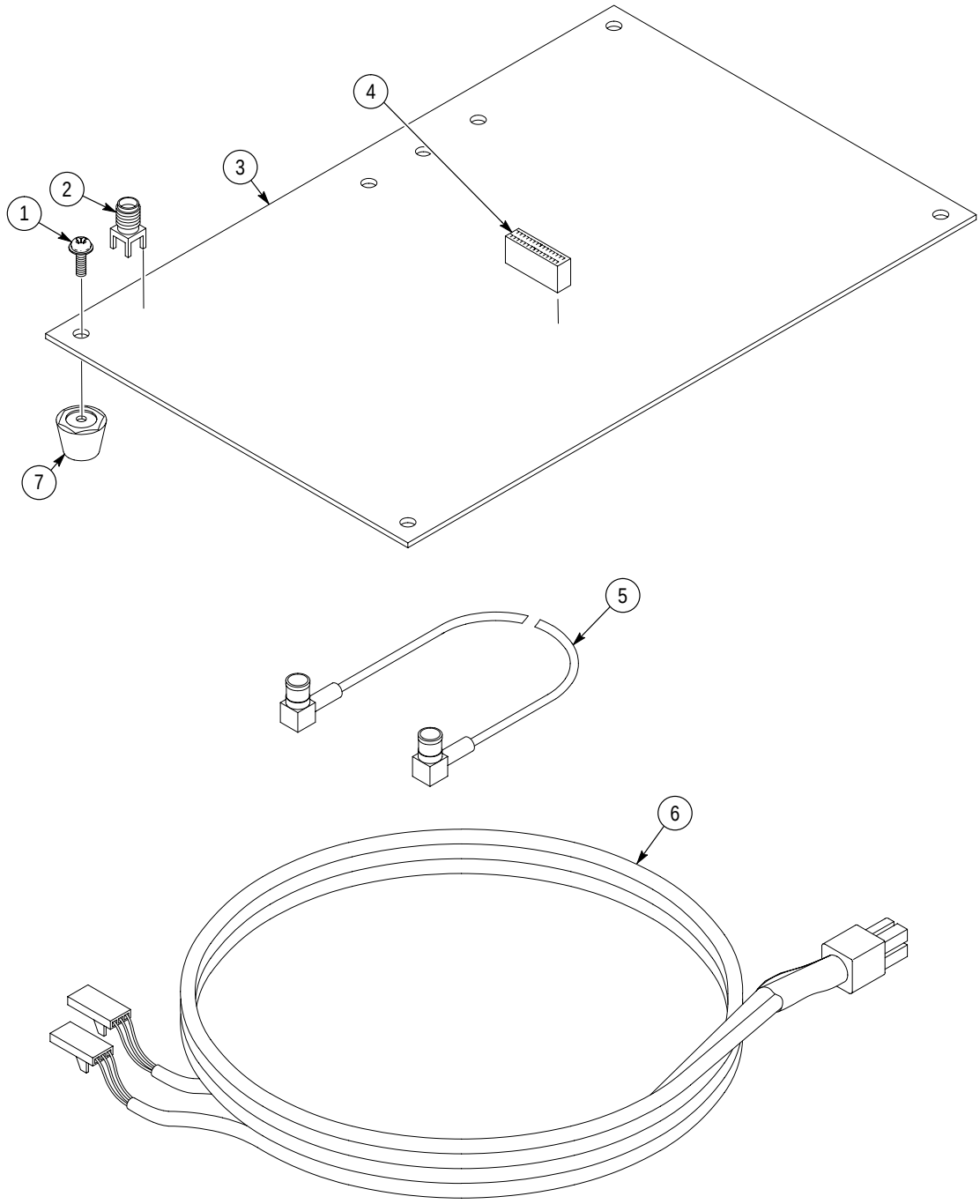


Figure 2: Exploded view

Appendix A: P6467 High-Speed Probe Adapter Input Connector

The flexible leads of the P6467 High-Speed Probe Adapter connect to a connector on the system-under-test. The mating connector is a 30-pin 0.05-inch x 0.1-inch AMPMODU System 50 connector and is available in a surface-mount version (AMP part number 104550-4) or a through-hole version (AMP part number 104078-4). Table 15, on the page 64, shows the pinouts of the connector on each P6467 Probe. The definition of the data pins depend on the 92A96 Probe Cable connection.

Table 15: P6467 Probe Pinouts

Buffer Assembly Pins	92A96/C96 Orange Probe	92A96/C96 Green Probe	92A96/C96 Blue Probe	92A96/C96 Gray Probe
Clock Pins				
2	Clk0	Clk1	Clk2	Clk3
Data Pins				
1	C0-7	C1-7	C2-7	C3-7
3	C0-6	C1-6	C2-6	C3-6
5	C0-5	C1-5	C2-5	C3-5
6	C0-4	C1-4	C2-4	C3-4
7	C0-3	C1-3	C2-3	C3-3
8	C0-2	C1-2	C2-2	C3-2
9	C0-1	C1-1	C2-1	C3-1
11	C0-0	C1-0	C2-0	C3-0
12	A1-7	A3-7	D1-7	D3-7
13	A1-6	A3-6	D1-6	D3-6
14	A1-5	A3-5	D1-5	D3-5
15	A1-4	A3-4	D1-4	D3-4
17	A1-3	A3-3	D1-3	D3-3
18	A1-2	A3-2	D1-2	D3-2
19	A1-1	A3-1	D1-1	D3-1
20	A1-0	A3-0	D1-0	D3-0
21	A0-7	A2-7	D0-7	D2-7
23	A0-6	A2-6	D0-6	D2-6
24	A0-5	A2-5	D0-5	D2-5
25	A0-4	A2-4	D0-4	D2-4
26	A0-3	A2-3	D0-3	D2-3
27	A0-2	A2-2	D0-2	D2-2
29	A0-1	A2-1	D0-1	D2-1
30	A0-0	A2-0	D0-0	D2-0
Ground Pins				
4, 10, 16, 22, 28				

Appendix B: P6467 Test Board

This appendix describes the P6467 Test Board. Use the test board to check the functionality and the performance of the P6467 High-Speed Probe Adapter as described in the *Performance Verification* chapter on page 37.

The P6467 Test Board is designed to accept a clock signal and data signals from a test generator and route them to a 30-pin connector to one of the flex leads of the P6467 Probe. Each of the data signals connects to two data channels at the 30-pin connector. Figure 15 shows the test board and the connectors.

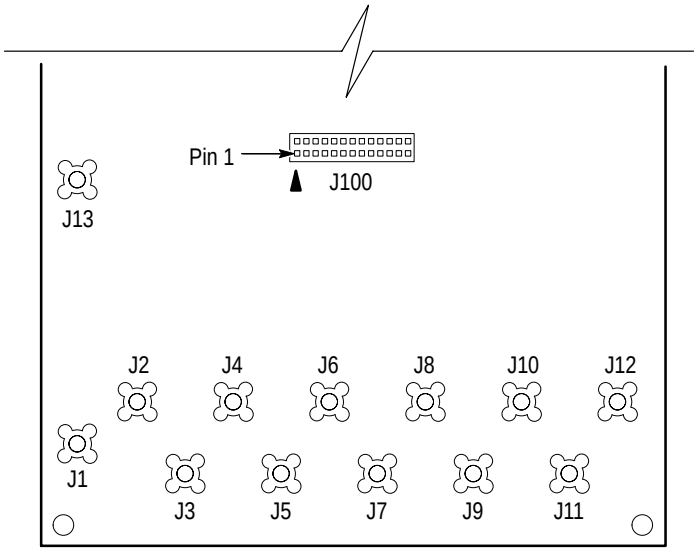


Figure 15: P6467 Test Board

The P6467 Test Board has room for additional components that are not installed. These components are only intended for use at the factory and are not required for the tests described in this manual.

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